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New Methodology for 25+ Gbps Connector Characterization

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Abstract

This paper presents several new findings in characterizing connector, via and PCB. It is shown that reducing the skew can improve a channel's insertion-loss-to-crosstalk-ratio (ICR). A board with a high-density BGA connector and two 6" traces was carefully laid out and built with flat-weave Megtron-6 material to optimize the channel's performance for 25+ Gbps. The two 6" trace models were extracted by a new de-embedding tool that matches both frequency- and time-domain responses through optimization. This allows the connector-only data to be extracted from a large board and compared directly with simulation results by a 3D field solver. The via was simulated with frequency-dependent dielectric constant and "wicking" effect (i.e., protrusion into the dielectric). It is shown that a smooth via with effective diameter could be derived to give similar impedance and delay with much less memory and CPU time in simulation. Finally, data are presented to show excellent correlation between simulation and measurement in connector, via and PCB.

Authors Biography

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Ching-Chao Huang, president of AtaiTec Corp., has more than 25 years of high-speed connector, package and system design, and SI software development experience. He held such positions as advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member, and he has many patents and publications. Dr. Huang received his BSEE from National Taiwan University, and MSEE and PhD from Ohio State University.

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Introduction

A connector usually accounts for the biggest impedance discontinuity and crosstalk source in chip-to-chip interconnect. To properly characterize a high-speed mezzanine connector (IT5), the test vehicle must be so designed that measurement data are not corrupted by PCB variation. Simulation models must resemble the test vehicle in dimensions and PCB material properties. To extract and characterize the connector and vias from the test vehicle, one also needs accurate de-embedding tools. This paper examines the PCB construction and its effect on overall channel performance. Several new methodologies are presented that help achieve good correlation between simulation and measurement.

An initial test vehicle was fabricated to highlight the performance of a high speed differential connector. However, the measurement data had much more degradation when compared to initial simulated data. By using the methods covered in this paper, a new and improved test vehicle was fabricated. The new test vehicle's data had significant improvement between initial simulation data, and measured data. As shown in Figure 1, each test vehicle is composed of a motherboard and a daughterboard that are connected at the center through an IT5 mezzanine connector. Up to 15 differential pairs can be measured with each test vehicle.

Both motherboard and daughterboard PCBs have vertical mount SMA launches that connect to 6" differential stripline traces. The first (or old) PCBs have 30 copper layers with Reverse-Treated Foil (RTF) copper and FR408 dielectric material. The second (or new) PCBs have 26 copper layers with Hyper Very Low Profile (HVLP) copper and Panasonic's Megtron 6 dielectric material. In addition to the dielectric material and copper profile, the glass weave style has been changed to improve the channel's overall performance. The old PCBs use a 1080 style weave, which is a commonly used glass weave style. The new PCBs use a combination of 3313 and 2-ply 1078 glass weaves to improve overall dielectric uniformity within each stripline differential pair.

Figure 2 shows the measured vs. simulated ICR (insertion-loss-to-crosstalk ratio) for both test vehicles. The ICR curve is a metric found in IEEE's 802.3ap specification [1] that compares the signal's loss and unwanted noise in a channel. All ICR curves in Figure 2 include SMA launches, stripline traces, connector vias, and the IT5 mezzanine connector. Simulation for the old test vehicle passes the extrapolated ICR specification up to 19 GHz. However, the old measurement data only pass up to 11 GHz. This large discrepancy is attributed to poor PCB fabrication and material performance.

The simulation and measurement data of new PCBs correlate very well. Simulation models do not account for the wide variety of fabrication variation. To reduce channel degradation due to fabrication variation, PCBs must be designed carefully beforehand. Large improvement in the measured channel performance of new PCBs, as shown in Figure 2, is the direct result of using better material and PCB design guidelines. The rest of the paper will show how the new test PCBs were designed and validated using new de-embedding tools and new validation methods.

Figure 1. Test vehicle with IT5 mezzanine connector.

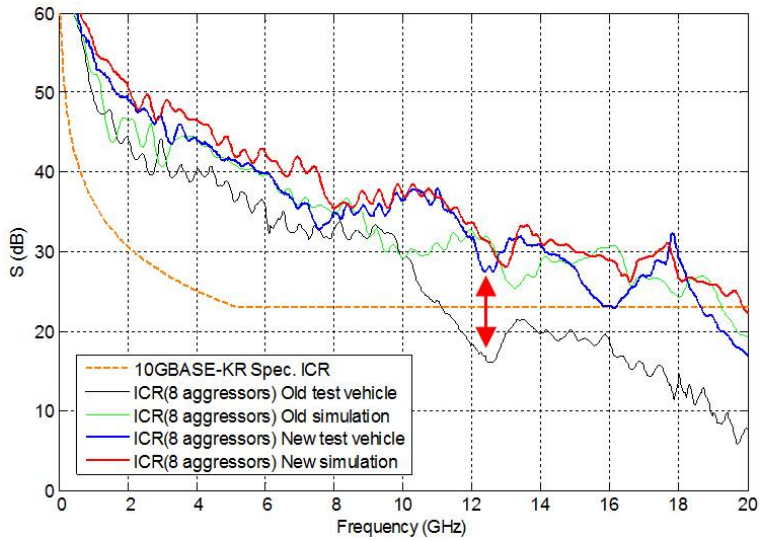

Figure 2. ICR curves for two test vehicles.

PCB material selection

The PCB material is an important factor in designing 25+ Gbps channels. It determines the overall signal attenuation of a channel as well as the integrity of measured data. Using a low-loss dielectric in combination with a flat glass weave will improve channel performance greatly. There are a variety of glass styles one can choose from. There are also many variations in resin content versus glass. In this study the 1080 and 1078 weave styles are compared.

Glass weave effect on intra-pair skew

The fiber bundles in the 1080 weave style are tightly wound, producing large resin pockets and areas with “ropes” of glass weave. Consider the case in Figure 3 where a stripline differential pair is routed with one stripline on top of the resin pockets and the other stripline above the glass ropes. Typically, resin has a dielectric constant of around 3, whereas PCB glass is around 5 to 6 depending on the manufacturer. Given the difference in the dielectric constant for each material, the stripline that “sees” more epoxy resin will have higher impedance, and the stripline that sees the glass ropes will have lower impedance. Since propagation delay is dependent on the effective dielectric constant the trace sees, each stripline will end up having a difference in delay. This difference in delay will cause intra-pair skew in the differential pair. Intra-pair skew can significantly degrade channel performance in differential insertion loss and crosstalk.

In the case of the 1078 weave, the glass fiber bundles are spread out, resulting in an even distribution of glass across the surface. Since the gaps in the PCB glass are now reduced, each individual stripline will see a much more uniform dielectric constant, which leads to matched delay and overall minimized intra-pair skew.

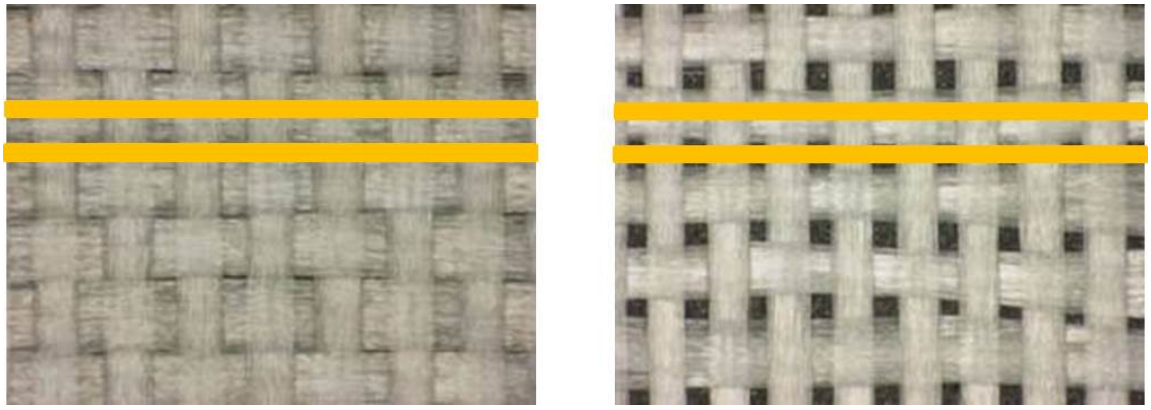

Figure 3. 1078 style weave (left) and 1080 style weave(right) with differential stripline.

In time domain (Figure 4), there is a large discrepancy in single-ended impedance (at 20/80 rise time of 50ps) between two stripline traces in the 1080 glass weave case. The higher the impedance a trace sees, the faster the signal will propagate (due to more resin and less glass). As a result, around the connector via region, the two single-ended signals arrive at different times, causing intra-pair skew. In the case of the 1078 glass weave, the impedance profiles for both single-ended striplines are very similar. Since both striplines’ propagation speeds are about the same, they reach the connector via at around the same time.

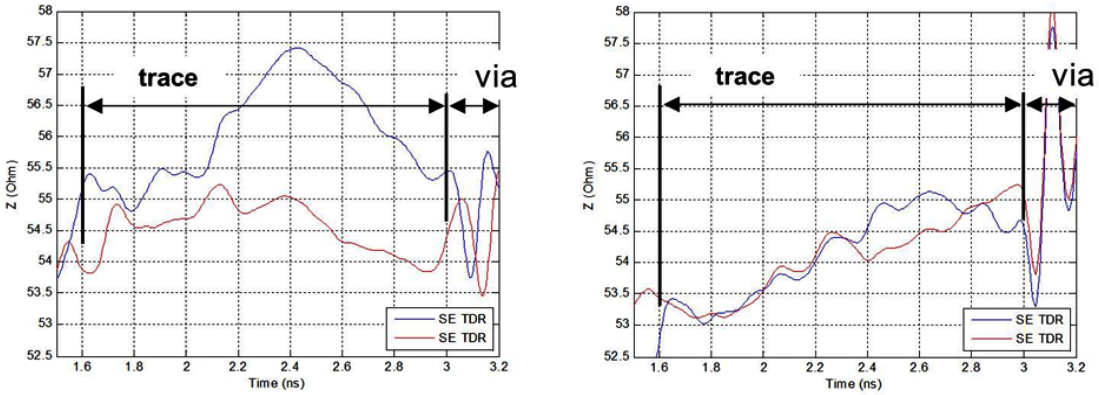

Figure 4. Single-ended impedance curves for 1080 (Left) and 1078 (Right).

The intra-pair skew will translate into degradation in differential performance. Figure 5 shows the degradation in differential insertion loss and far-end crosstalk with ~30ps of skew in the channel. After the intra-pair skew is corrected, significant improvement in differential insertion loss and far-end crosstalk is observed. In order to achieve good channel performance and correlation, it is crucial to design PCBs with in-depth material and fabrication knowledge to minimize the intra-pair skew.

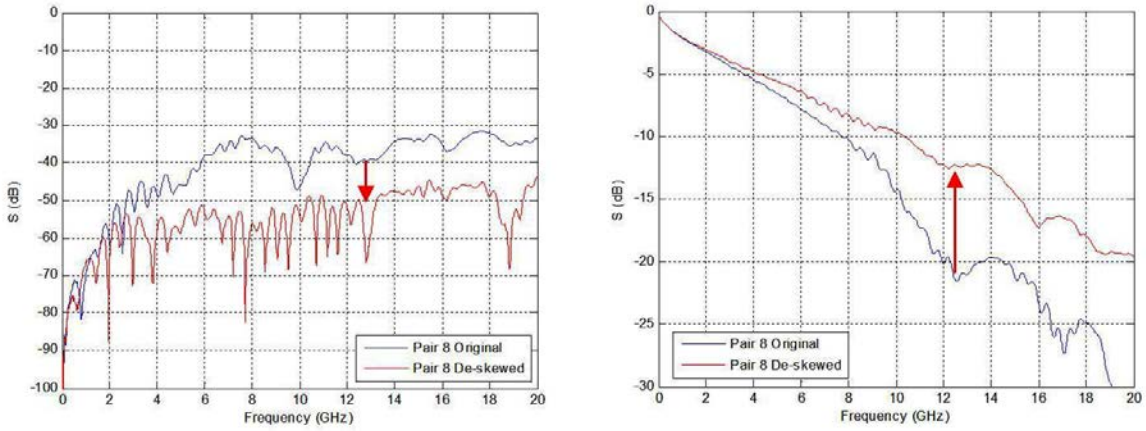

Figure 5. IL and FEXT before and after de-skewing.

Conductor and dielectric losses

To ensure good channel performance at 25+ Gbps, one must understand the properties of copper and dielectric material and control the signal's attenuation. Many types of copper profiles exist in today's market, including Reverse-Treated-Foil (RTF) copper, Very Low Profile (VLP) copper and Hyper Very Low Profile (HVLP) copper. All these types have different conductor loss properties as well as cost. If the attenuation is not accurately predicted in the design stage, the channel's eye width and height could be very different from simulation. PCB dielectric material can also vary greatly in dielectric constant and

loss. For example, typical FR408 material can have a loss tangent around 0.015 and a low-loss dielectric can have a loss tangent of 0.005.

In order to predict the total loss of a channel, one must accurately compute the conductor and dielectric losses. A Microsoft Excel based loss calculator [2] has been proposed to IEEE 802.3bj to model conductor and dielectric losses in a stripline channel. It has default data for Megtron-6, FR408 and Nelco N4000-13SI material. These data include frequency-dependent dielectric constant and dielectric loss values up to 20 GHz. Once the user specifies the trace length, dielectric thickness, and trace dimensions, the calculator will give an estimated insertion loss curve for the channel. In addition, there are three choices for copper roughness: low, medium, and high.

To test the accuracy of this calculator, two 6-inch-stripline-only measurements were extracted from both old and new test vehicles. Table 1 gives the general construction for each test vehicle, and cross sections of RTF and HVLP are shown in Figure 6. Figure 7 shows the measured vs. estimated loss for both test vehicles. The estimated loss was computed by [2], using pre-defined FR408 and Megtron-6 parameters in conjunction with the selection of high roughness for RTF copper and low roughness for HVLP copper. The measured and estimated losses track each other in general.

Design category	Old test vehicle	New test vehicle
Copper profile	RTF	HVLP
Dielectric material	FR-408	Megtron 6
Glass weave style	1080	3313/1078
Backdrill	Yes	Yes
Trace length	6"	6"
Copper layers	30	26

Table 1. Comparison of two test vehicles

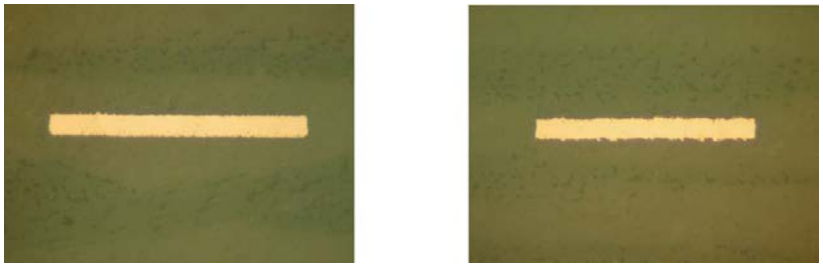

Figure 6. HVLP (left) and RTF (right) copper profiles.

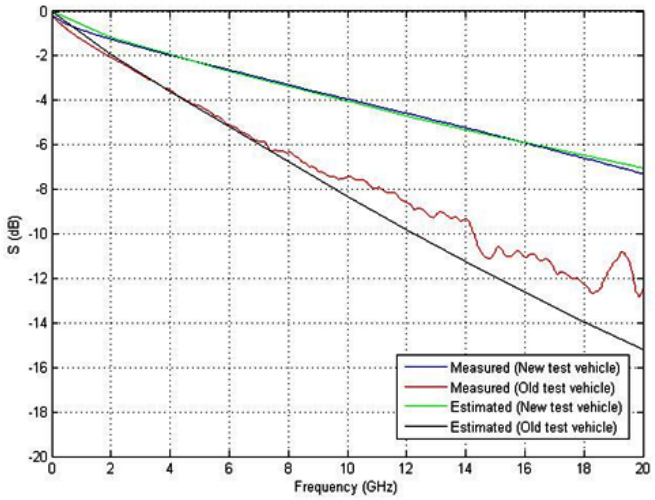

Figure 7. Measured vs. estimated loss.

Frequency-dependent DK extraction

FR408 and Megtron-6 are common PCB dielectric materials, but not every PCB will use these two materials. In addition, the PCB glass weave style can change the effective dielectric constant of that material due to the different distribution of PCB glass. The method being proposed below can effectively extract frequency-dependent dielectric constant values for any material that can support a stripline structure. This proposed method requires an accurate de-embedding tool in order to get reliable data. A new tool is introduced in the next section for such accurate de-embedding.

In-Situ De-embedding

In-Situ De-embedding (ISD) is a new de-embedding software program from AtaiTec [3]. It removes the effect of test fixture (SMA connector + lead-in traces) and extracts the S-parameters of DUT (device under test). Some of this tool's features are the following.

- ISD requires only a 2x length thru test coupon, but it does not require that the 2x thru and DUT boards have the same impedance. It is because ISD uses the test coupon only as a reference for frequency- and time-domain optimization, not for direct de-embedding.
- ISD only requires two Touchstone files to run: a 2X thru length measurement file and a SMA-to-SMA DUT board measurement file. Once the user has input these files, ISD will automatically de-embed out the SMA and lead-in traces of the DUT board. ISD will output three Touchstone files for: de-embedding from the left, de-embedding from the right and the DUT itself.
- Figure 8 shows an example where the DUT impedance is causal after ISD, but non-causal after such conventional calibration as TRL. The conventional method

is more prone to non-causal results, mainly caused by differences between the calibration and actual DUT boards.

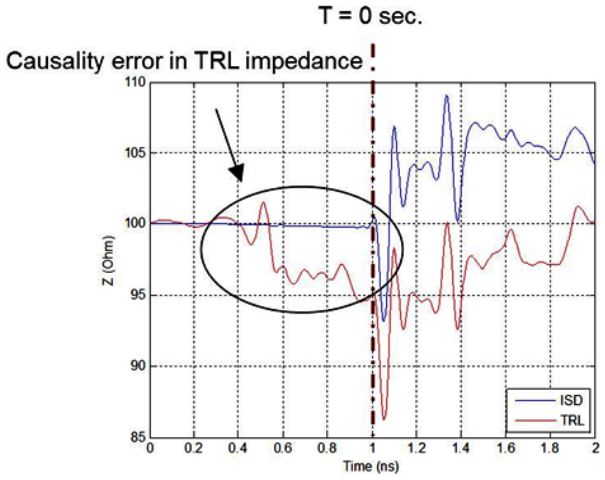

Figure 8. DUT impedance after ISD and TRL.

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DK Extraction

Extracting a frequency-dependent dielectric constant accurately requires stripline-only measurement. The stripline-only measurement needs to be free of any impedance discontinuities caused by the SMAs or the SMA vias. Since ISD removes the impedance discontinuities of all incoming traces and launches for the DUT board being measured, the leftover DUT results are quite accurate. In this study, a 6 inch stripline trace is extracted. To achieve this, a 6 inch and a 12 inch striplines on the same layer are constructed. The 6 inch stripline is used as the 2X thru to de-embed the 12 inch stripline. As shown in Figure 9, ISD will de-embed starting from each SMA, leaving 6” stripline for the DUT itself. Each of the left and right de-embedding files consists of SMA, SMA via, and 3 inches of stripline.

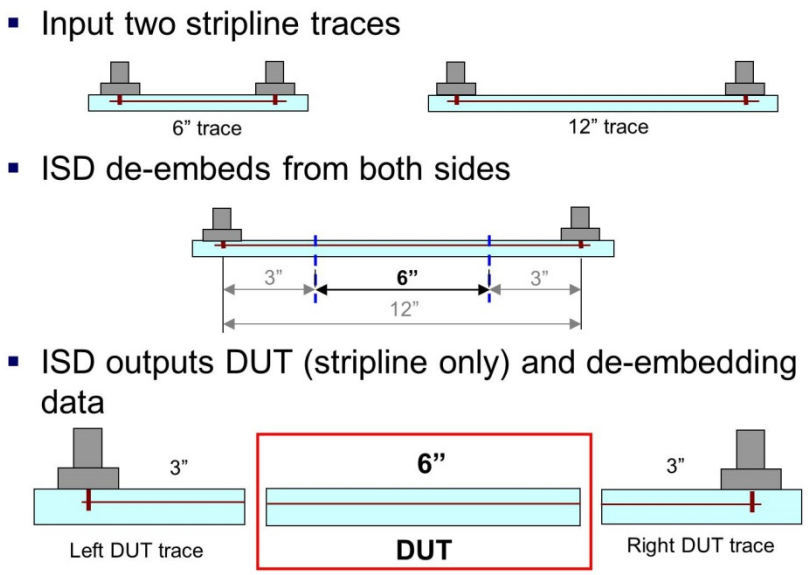


Figure 9. Using ISD to extract a 6" trace-only model.

Now that there are 6-inch-stripline-only measurement data, the next step is to back calculate the effective dielectric constant of the material the stripline is in. Noting that the signal's propagation speed is simply the length divided by phase delay in the absence of discontinuities, one can compare the signal's propagation speed (v) and the speed of light (c) to derive the frequency-dependent effective dielectric constant (ε) through:

$$v = \frac{c}{\sqrt{\varepsilon}}$$

Table 2 shows the frequency-dependent values from 200 MHz to 20 GHz.

Frequency (GHz)	DK
0.2	3.736
1.15	3.6097
2	3.583
5	3.548
10	3.526
20	3.519

Table 2. Frequency-dependent effective dielectric constants

Verification of PCB structure

The PCB fabrication process, while having been refined over the years, can still have variation in via and trace structures. The actual structure must be verified to ensure that simulation models are using the same geometry.

Cross-sectioning of vias

After the new test vehicle was fabricated, cross-sections were taken of a differential pair of vias (Figure 10). Such parameters as via diameter, via pad diameter, via position, copper layer mis-registration and dielectric thickness were measured and were found to have only little difference from the simulation models.

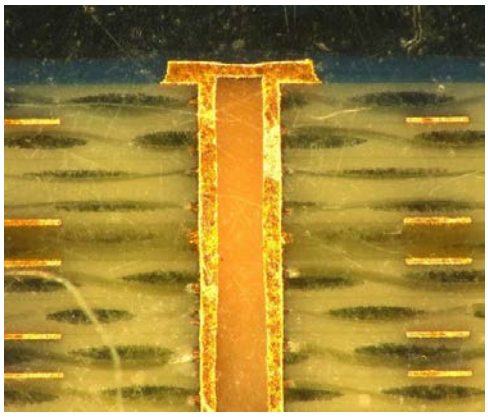


Figure 10. Via's cross section.

Copper wicking

Copper wicking (Figure 11), which corresponds to small protrusions from the via wall, is observed. These protrusions seem to track the glass fibers that intersect the via wall. Copper can migrate along the glass fibers when the epoxy resin is damaged or separated from the glass fibers. The epoxy resin can be damaged due to drill wandering or during the lamination process. In the new test vehicle, copper wicking of ~20 microns is observed. For comparison, IPC defines class 3 (the most stringent specification) copper wicking to be no larger than 80 microns [4].

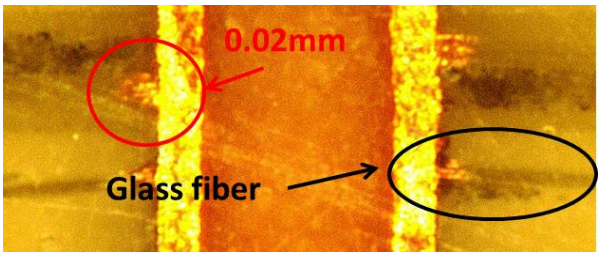


Figure 11. Copper wicking.

Since the new test vehicle is fabricated to handle 25+ Gbps data rate, the copper wicking's signal integrity impact is studied. Measurement data are de-embedded to include only the vias and a small section of microstrip trace. Three simulation models are created to observe the effect of copper wicking. The base case, a 10 mil via, corresponds to the vias without copper wicking. The 2nd simulation model, with concentric rings of 100 microns pitch protruding 20 microns from the via wall, represents the exact structure. The last simulation model, a smooth via of 10.6 mils diameter, is intended to capture the wicking effect without including the fine details of concentric rings. Table 3 compares the memory and CPU time requirements in simulating these models in HFSS [5].

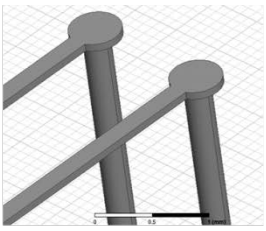
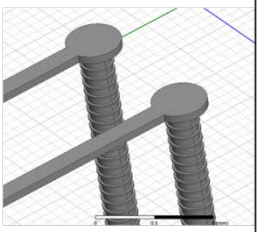
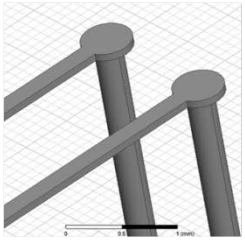
Model	 Smooth 10.0 mil via	 Ring model	 Smooth 10.6 mil via
# of mesh	879212	3145934	881926
RAM	9.98 GB	40.1 GB	9.98 GB
Time	1:14:43	4:23:02	1:15:51

Table 3. Copper wicking simulation models.

Figure 12 shows good correlation among the ring model, the 10.6 mil effective via model and the measured data. It is now apparent that, for accurate and efficient via simulation, the via's diameter can be slightly enlarged to account for the wicking effect.

Note that impedance can differ by ~2 ohms (at 30ps rise time) with or without 20 microns of copper wicking. If a board is fabricated with 80 microns of copper wicking, the difference in impedance will be even larger.

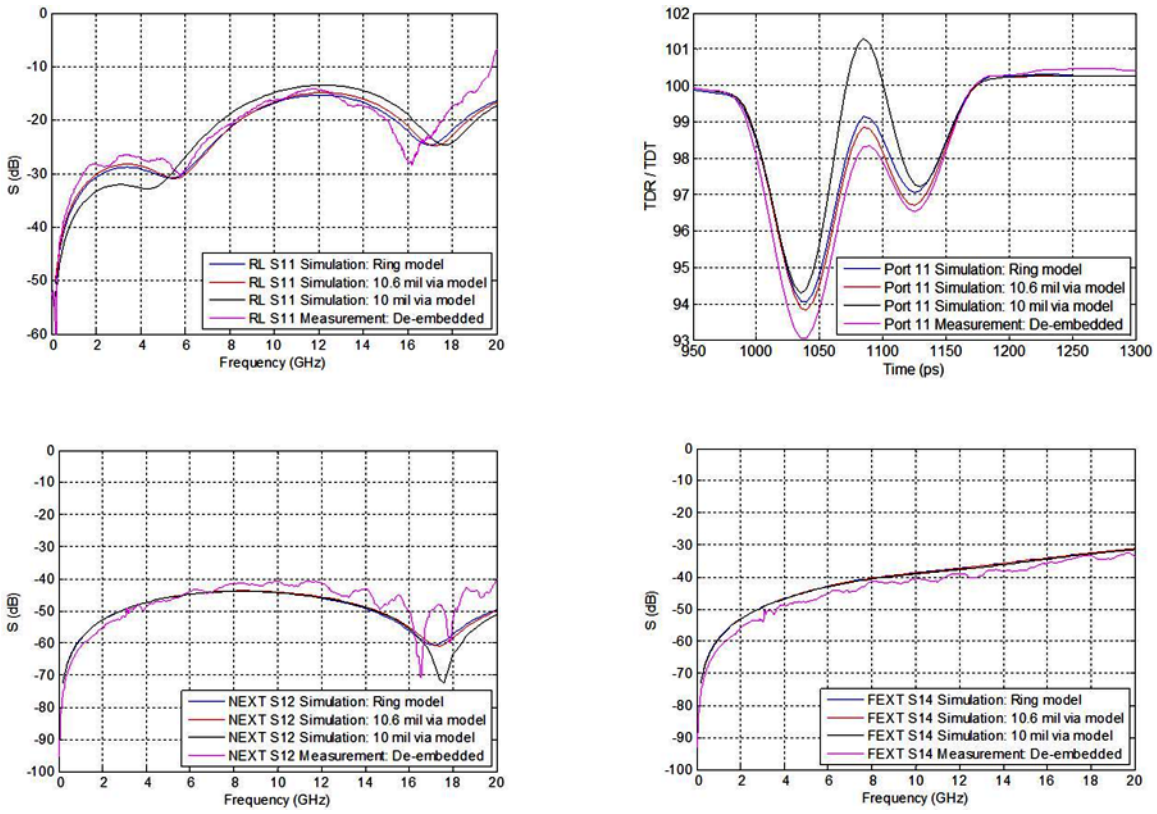


Figure 12. Via's simulation vs. measurement.

Channel's performance

The insertion loss to crosstalk ratio (ICR) is an important measure to determine if a channel will perform at 25+ Gbps. Simulation will be correlated with measured ICR for both the full channel and connector + via only data. Good correlation is an indication that the simulation, design and extraction methodologies are working as intended.

Full channel correlation

The PCB trace model is one of the biggest variables in correlating simulation and measurement in a full channel (Figure 13). No simulation model can duplicate the random effect of glass weaves and manufacturing variation. This paper takes a new approach in full channel correlation by cascading the simulated connector and via models with the ISD extracted SMA and trace model.

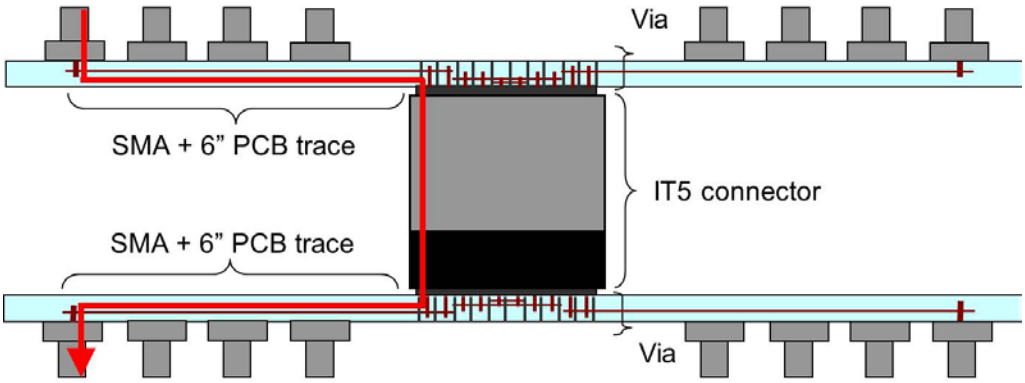


Figure 13. Full channel with IT5 mezzanine connector.

Figure 14 compares the measured vs. “simulated” full channel’s differential impedance where the “simulated” model is composed of the ISD extracted SMA + trace model in cascade with the HFSS simulated IT5 connector + via model. The randomness of PCB trace impedance is clearly seen in Figure 14 which is extracted by ISD. The only difference between measurement and simulation in this full channel is in the region of IT5 connector + via.

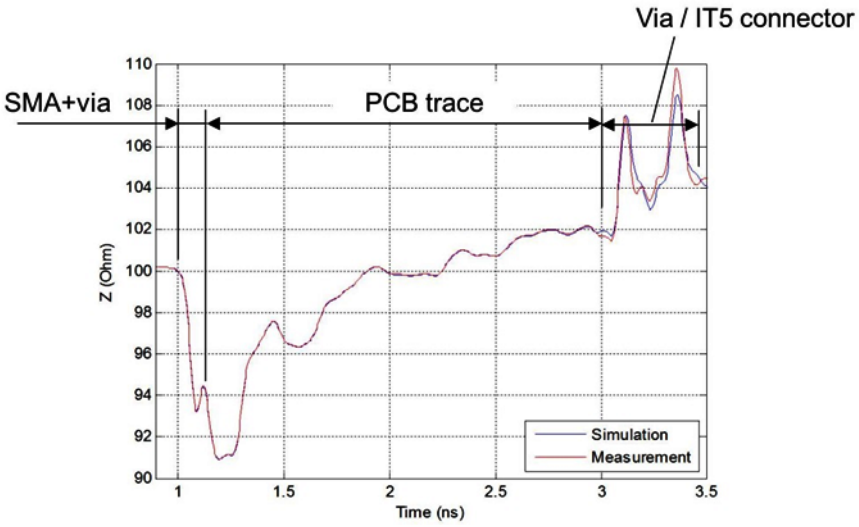


Figure 14. Differential impedance of full channel at 30ps rise time (20% to 80%).

Figure 15 shows good correlation between measured vs. simulated full channel’s differential insertion loss (IL), return loss (RL), near-end crosstalk (NEXT) and far-end crosstalk (FEXT).

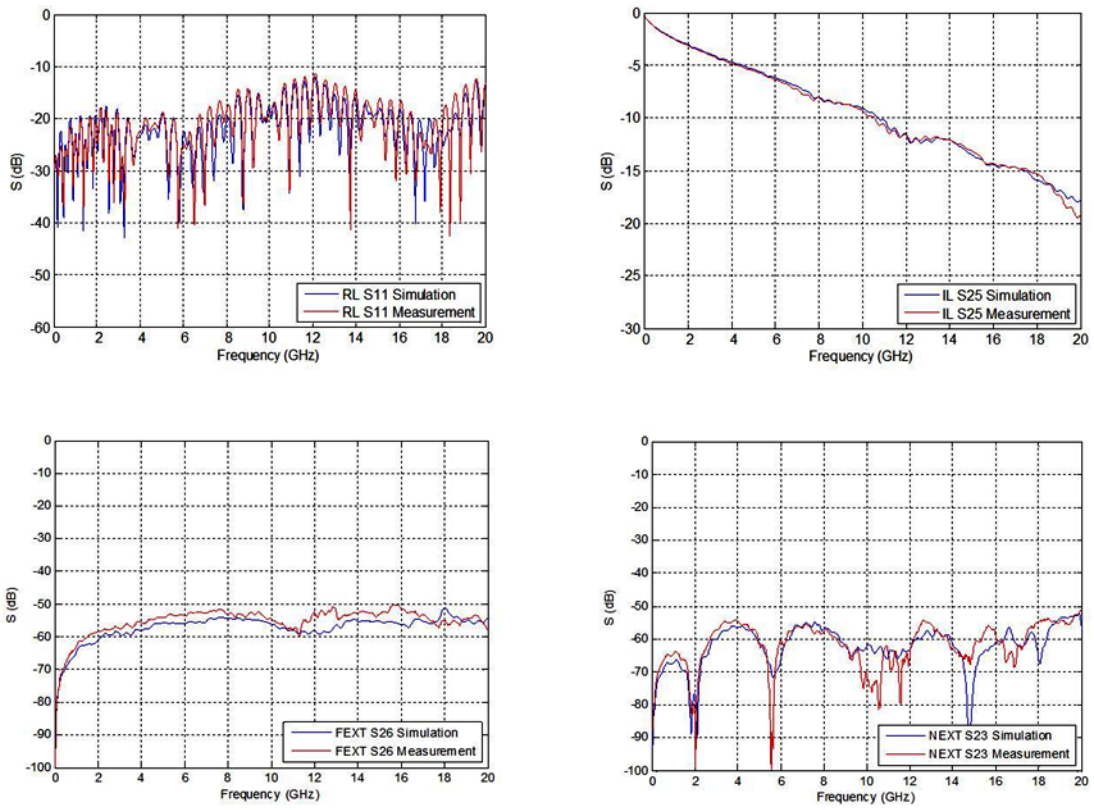


Figure 15. Differential IL, RL, NEXT and FEXT for the full channel.

Figure 16 also shows good correlation between simulated and measured ICR for the full channel. It confirms the channel's performance for 25+ Gbps.

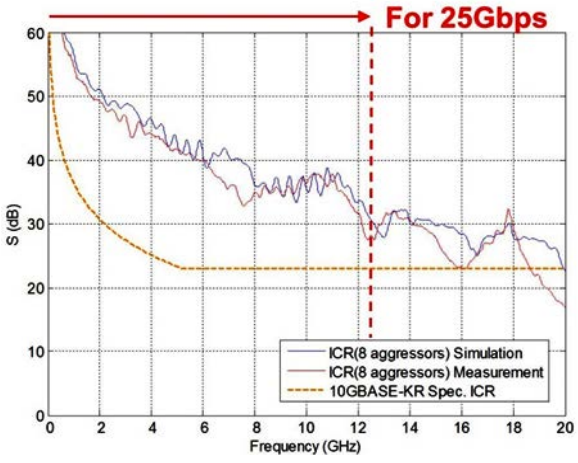


Figure 16. ICR for the full channel.

Connector and via characterization

The connector and via often account for the biggest discontinuity and crosstalk source in a whole channel. To understand the channel's limitation, one needs to also understand the connector and via performance in a practical channel environment. This paper shows key elements of PCB design which may affect the channel performance and a new procedure of characterizing connector and via from a large demo board (Figure 17). A large "demo" board is usually built and readily available to demonstrate the component's performance in actual operation. Being able to extract DUT from a large board helps us identify what causes the difference between the simulated channel performance at the design stage and measured channel performance after fabrication.

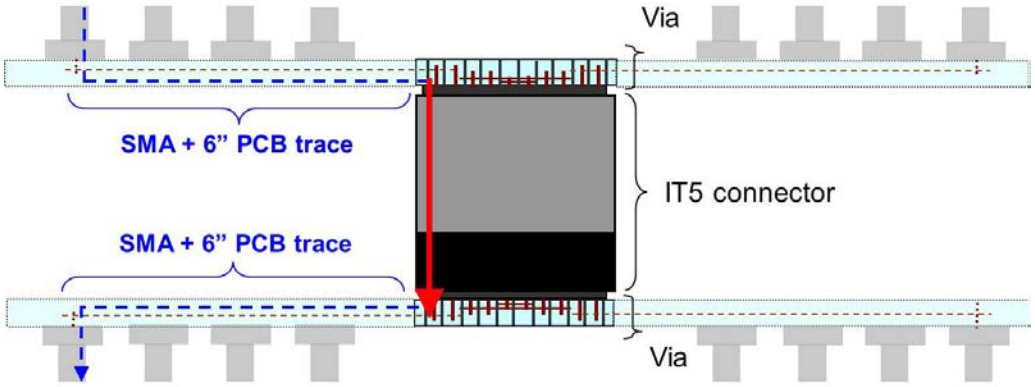


Figure 17. Using ISD to extract connector and via from a large board.

Figure 18 shows the connector and via's TDR impedance in a full channel vs. after de-embedding. More details are seen after de-embedding because more high-frequency signals remain. Good simulation vs. measurement correlation is achieved for the DUT (i.e., IT5 connector + via) only, after de-embedding SMAs and PCB traces.

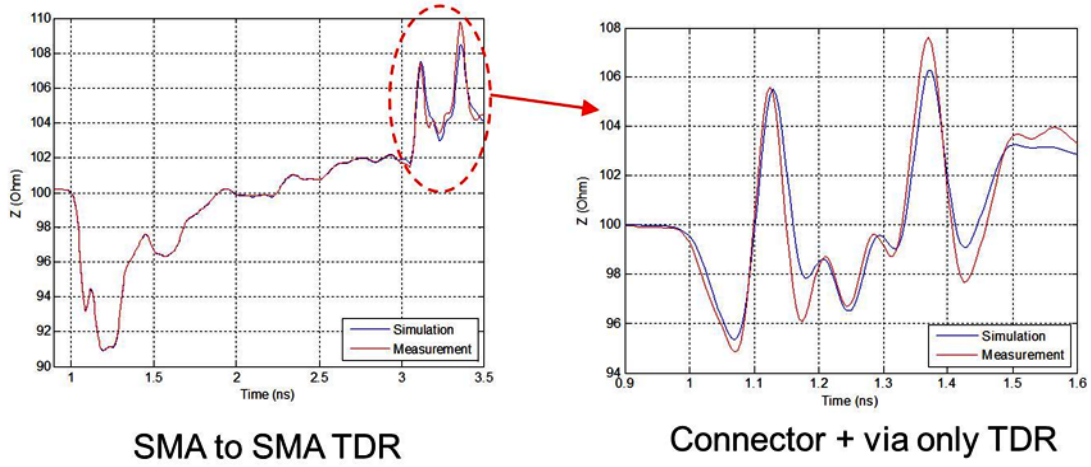


Figure 18. Connector and via's TDR impedance at 30ps rise time (20% to 80%).

Figure 19 shows the insertion loss (IL), return loss (RL), near-end crosstalk (NEXT) and far-end crosstalk (FEXT) of IT5 connector + via. The simulation vs. measurement correlation is again quite excellent, considering especially that the DUT is extracted from such a large board.

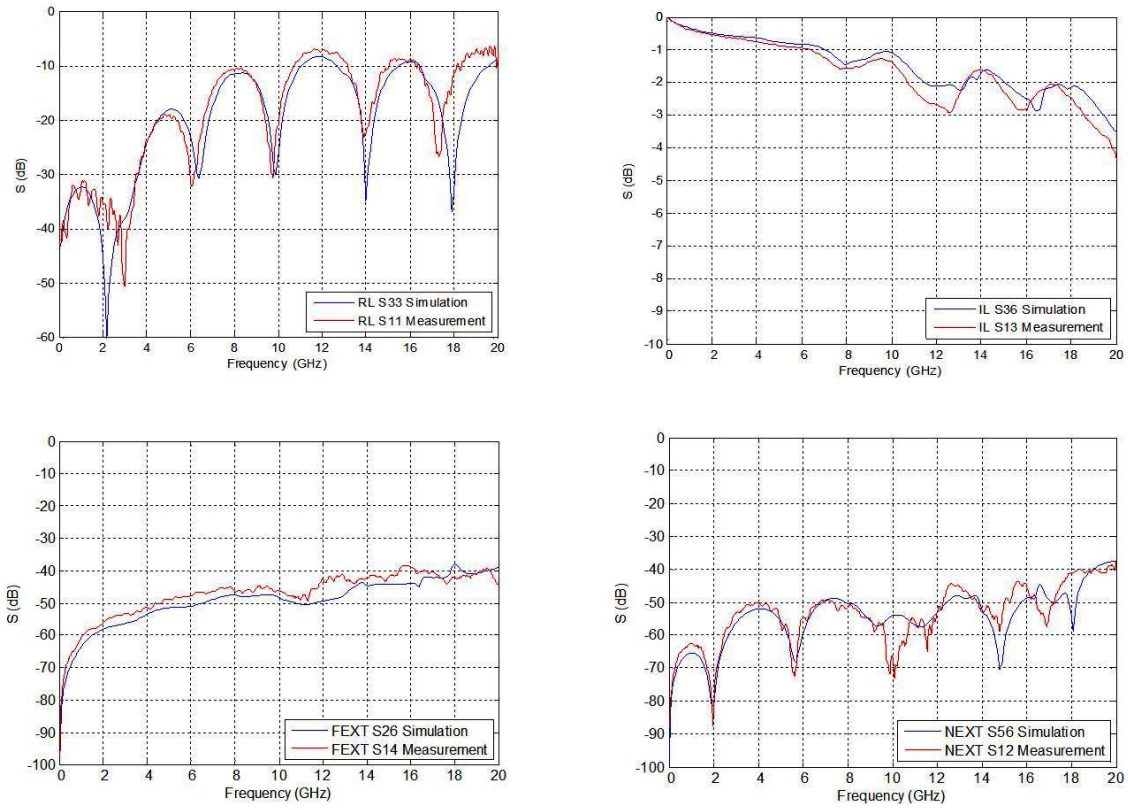


Figure 19. Differential IL, RL, NEXT and FEXT for only the connector and via.

Figure 20 shows simulated vs. measured ICR for the connector and via only where good correlation is again observed. Note the similarity in ICR between the full channel (Figure 16) and connector + via only (Figure 20). It is understandable in that most of the crosstalk is from the connector and via in this case and ICR (with respect to FEXT) is insensitive to attenuation.

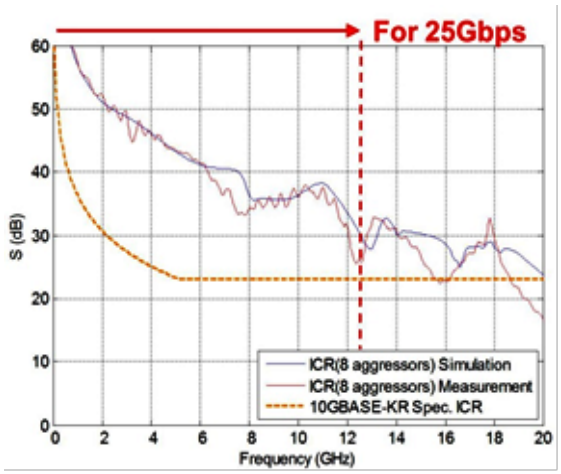


Figure 20. ICR of connector and via.

Conclusion

Several topics have been discussed in this paper:

- Glass weaves and their effect on skew
- Effect of skew on insertion loss and crosstalk
- Copper wicking and its effect on impedance
- In-Situ De-embedding (ISD) to extract DUT from a large board
- Stripline trace extraction for frequency-dependent DK calculation
- SMA and trace extraction for full-channel correlation

Two test vehicles were built to demonstrate IT5 connector's performance to 25+ Gbps in a channel. The newer test vehicle gave better performance through better material and design practice. Using ISD to extract accurate trace models, good correlation is achieved for both full channel and connector + via only TDR, S parameters and ICR.

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