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Embedded DC Blocking Capacitors in Connectors - Study of Impacts on PCB Design and High Speed Serial Link Performance

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Abstract

DC blocking capacitors and connectors are commonly used in today's multi-gigabit serial links. Capacitors can cause significant drops in channel impedance. To include capacitors on a PCB, vias are required to connect the inner layer to the top layer. The vias introduce more impedance discontinuities and can cause crosstalk to neighboring signal vias. Capacitors and vias consume valuable PCB real estate and routing space. These problems will be more critical as signaling speeds approach 25Gbps and signal density increases. To solve these problems, the capacitors are moved from the PCB into the connector, eliminating the need for capacitor vias. The capacitor geometry is modeled using a full wave solver and optimized for impedance and crosstalk. The effectiveness of this solution is evaluated by simulating and comparing a channel with capacitors mounted on the PCB and a channel with capacitors embedded into the connector. The results are verified by measurement of actual test vehicles.

Authors Biography

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Arai holds 15 US, and 19 Japanese patents. He received a BSME from Waseda University, Tokyo, Japan.

Ching-Chao Huang, president of AtaiTec Corp., has more than 25 years of high-speed connector, package, and system design and SI software development experience. He held such positions as advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member, and he has many patents and publications. Dr. Huang received his BSEE from National Taiwan University, and MSEE and PhD from Ohio State University.

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Introduction

DC blocking capacitors and high density connectors are commonly used in today's multi-gigabit chip-to-chip serial links. Electrical implementation agreements for 25Gbps and 28Gbps currently being defined by OIF and IEEE require DC blocking capacitors and can include up to two connectors. DC blocking capacitors are used to separate the different bias voltages of the transmitters and receivers. High density connectors are used to carry the high speed signals from one PCB to another, such as a line card to a backplane or a mother board to a mezzanine card, while allowing disconnection and connection when necessary. The DC blocking capacitors themselves can cause significant drops in channel impedance. In order to include DC blocking capacitors onto a PCB, vias are required to connect the inner routing layer to the top layer. These added vias introduce even more impedance discontinuities and can cause unwanted crosstalk to neighboring signal vias. Accurately modeling and optimizing the capacitor on the PCB with its vias can be a difficult task. Aside from impacts on signal integrity, DC blocking capacitors and their vias consume valuable PCB real estate and routing space. These problems will be more and more critical as signaling speeds approach 25Gbps and signal density continues to increase.

To solve these problems, the DC blocking capacitors are taken off of the PCB and embedded into the high density connector. This eliminates the need for DC blocking capacitor vias, which removes the impedance discontinuities and crosstalk that come along with them. It also simplifies the 3D geometry, which makes it easier to create an accurate model. The effectiveness of this solution is evaluated by simulating and comparing the performance of two channels. The first channel consists of on-board DC blocking capacitors and a conventional board-to-board connector. The second channel consists of a connector with embedded DC blocking capacitors. Everything else in the two channels is made equal. S-parameters and channel simulations are compared. Test vehicles for these two channels are built and measured to verify simulation results.

Capacitor characterization, modeling, and optimization

To optimize the design of a connector with embedded capacitors, a capacitor model is needed. All structures of the connector are known and can be modeled precisely except for the capacitor. A typical capacitor construction is shown in the Figure 1(a). It consists of external electrodes, thin plates of inner electrodes and a ceramic body. Dense inner electrodes are connected in parallel to provide a sum of capacitance as in Figure 1(b). One chip capacitor can consist of a thousand plates of inner electrodes. It is not practical to model such a 3D geometry in detail. Instead, an empirical approach is taken. A pair of 0402 chip capacitors is first characterized by way of measurement. Various geometries are then studied to find one that yields equivalent characteristics. Ansoft's 3D field solver, High Frequency Structure Simulator (HFSS), is used for this study. Once correlation is achieved, such a 3D geometry can be used with confidence for optimization and analysis.

A test PCB is used to characterize a pair of capacitors with a 1.5mm pitch. Short coplanar traces connect the capacitors to probe pads. The probe pads are placed far enough away that they do not disturb the impedance of the capacitors themselves. Probes

are used to take measurements on a Vector Network Analyzer (VNA). A picture of the test PCB and measurement setup are shown in Figure 2. No attempt is made at this point to optimize the capacitor footprint, as the capacitor sits above a solid ground plane.

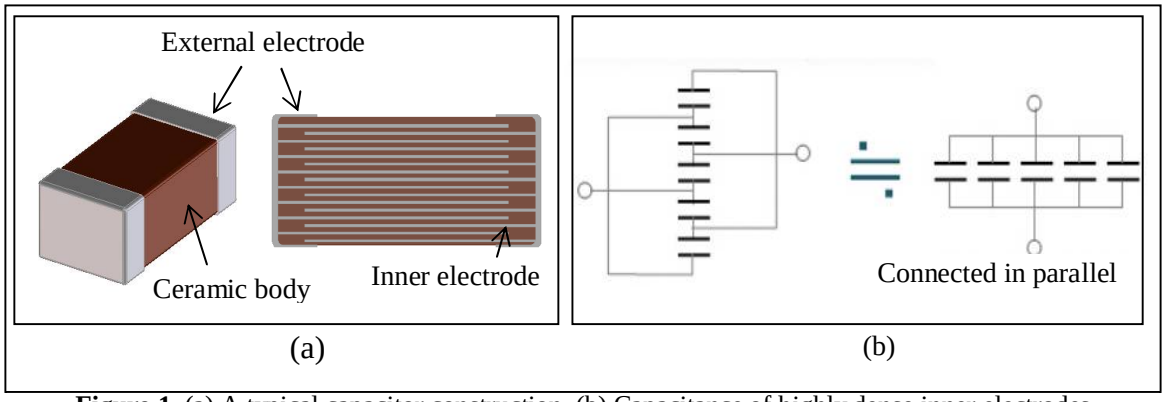


Figure 1 (a) A typical capacitor construction, (b) Capacitance of highly dense inner electrodes

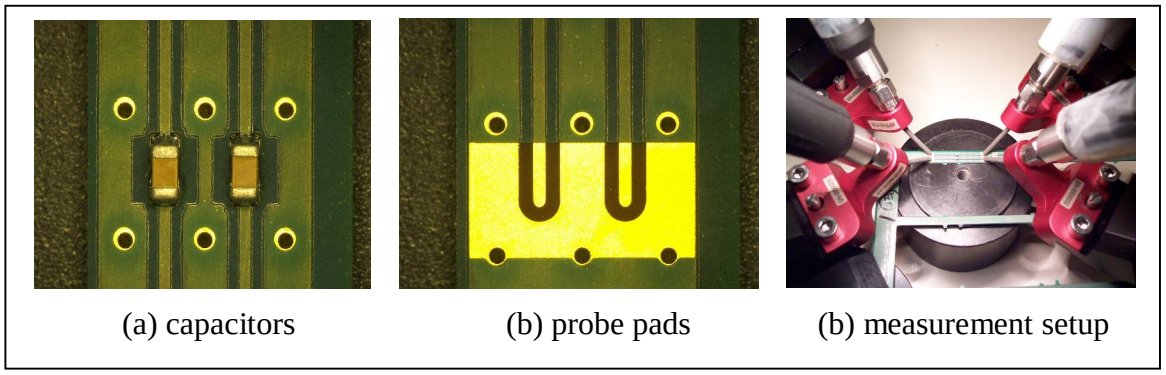


Figure 2 Test PCB and measurement setup for characterizing capacitors

The test PCB is modeled in HFSS. Lumped ports are used in order to mimic the effects of the probes. The simulation setup is shown in Figure 3. The dimensions of the external electrodes of the capacitors are known and are included in the model.

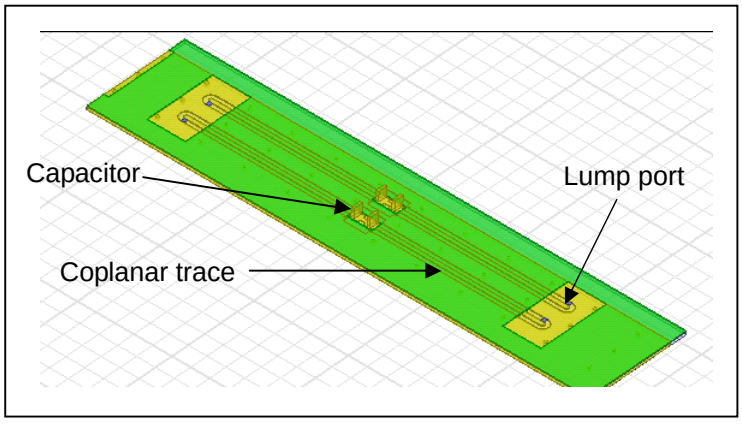


Figure 3 Test PCB simulation setup

The first 3D geometry simulated, Model 1 shown in Figure 4(a), consists of a surface trace connecting the two capacitor pads with a ceramic block sitting on top. The resulting S-parameters are converted into a TDR impedance profile using AtaiTec's Advanced SI Design Kits (ADK) [1] as shown in Figure 5. Compared to measurement, the impedance of Model 1 is 7 ohms lower. To bump up the impedance, the ceramic block is removed in Model 2 shown in Figure 4(b). The TDR profile shows that the impedance does indeed increase but is still 3 ohms lower than measurement. The 3D geometry of Model 3 is meant to give a better match to the internal structure of a capacitor. A capacitor consists of many thin metal sheets separated by thin layers of dielectric material; however, it would not be practical to try to construct these densely packed metal and dielectric layers in HFSS. Instead, a small metal block is used. It can be seen from the TDR profile that Model 3 is an effective way of modeling a capacitor as its impedance is within 1.2 ohms of measurement. One can further refine the geometry to get a better match, but for our purpose, Model 3 is sufficient.

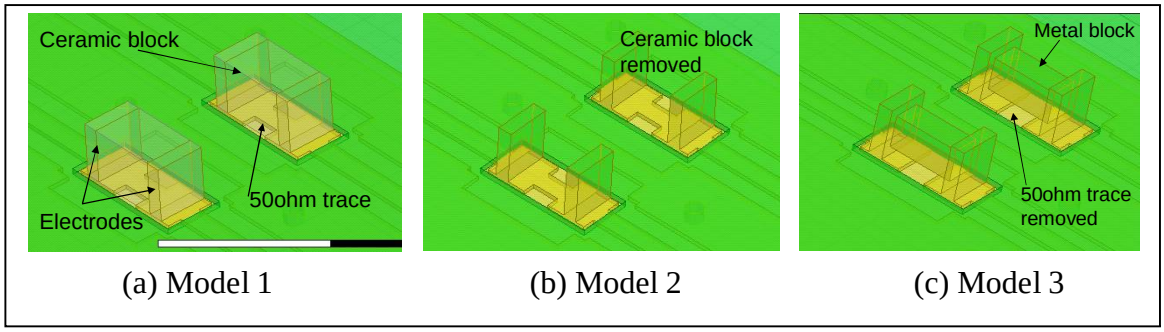


Figure 4 3D geometries used to model capacitor

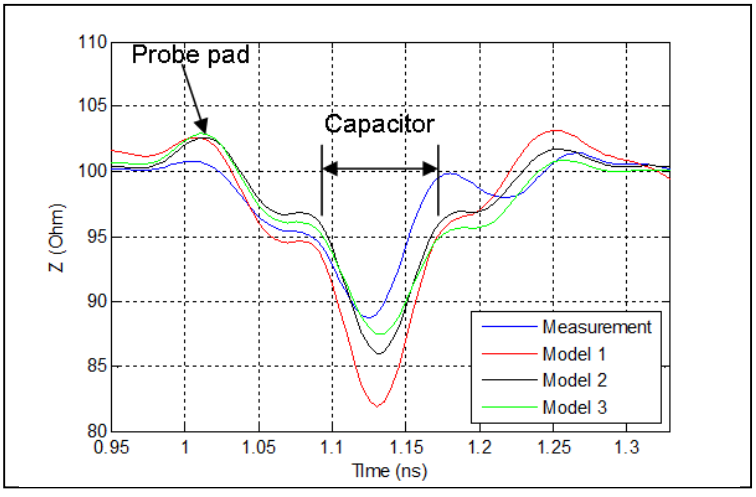


Figure 5 TDR profile @ 30ps rise time (20-80%) of capacitor measurement and Models 1-3

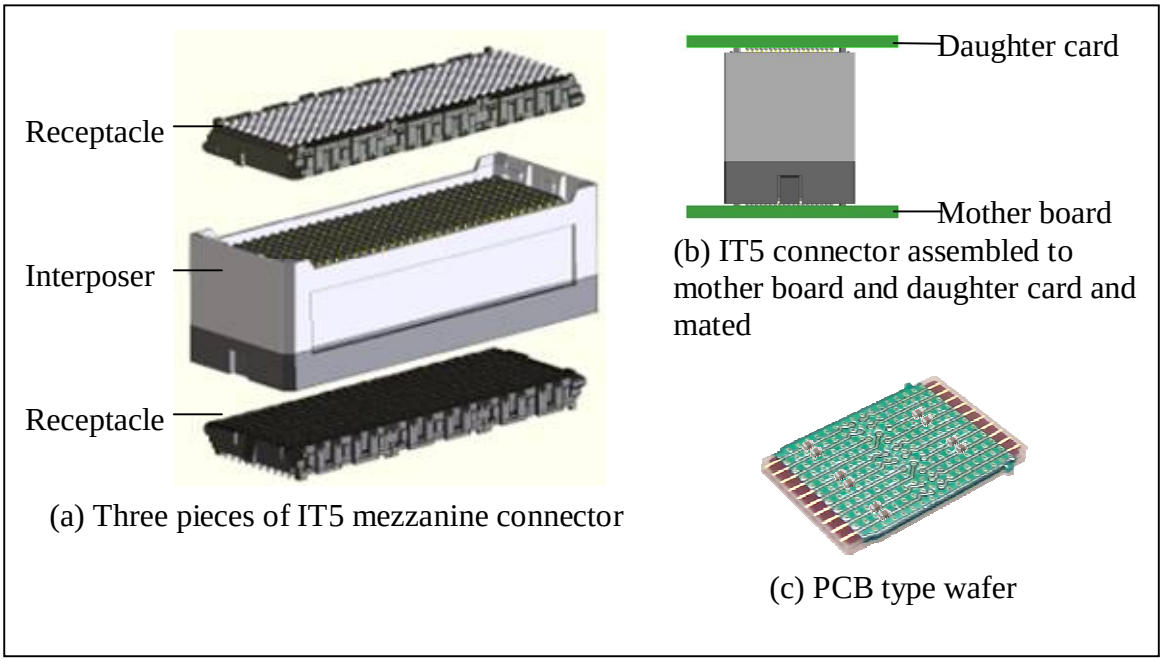
Embedded capacitor optimization

A high density mezzanine connector, Hirose's IT5, is used in this study. IT5 is a three-piece connector consisting of two receptacles and an interposer, shown in Figure 6(a). One receptacle mounts to the mother board with a ball grid array (BGA) attachment. The

other receptacle mounts to the daughter card, also with a BGA attachment. It utilizes the same reliable BGA technology and three-piece concept as described by Kikuchi et al[2]. The interposer mates with both receptacles to create a connection between mother board and daughter card. Figure 6(b) shows the IT5 connector assembled to a mother board and a daughter card and mated.

The interposer consists of multiple wafers, as many as thirty in one interposer, with five differential pairs per wafer. To be able to attach capacitors to the wafers, the wafers are fabricated using PCB technology. This allows the wafers to be panelized and enables a conventional surface mount technology (SMT) assembly process to be used for assembling the DC blocking capacitors. The capacitors are mounted on the top, with surface traces connecting the capacitors to the gold fingers. The use of only surface traces eliminates any via stubs. The PCB wafer can be seen in Figure 6(c).

The geometry of Model 3 of the previous section is used to optimize the footprint of the embedded DC blocking capacitor. It can be seen in Figure 5 that the capacitor tends to yield low impedance, 89 ohms in this case, if un-optimized. To counteract the capacitive impedance, cutouts are added to the ground plane underneath the capacitor pads to make the impedance more inductive. Figure 7 shows the ground cutouts and how they are aligned with the capacitor pads.



(a) Three pieces of IT5 mezzanine connector

(b) IT5 connector assembled to mother board and daughter card and mated

(c) PCB type wafer

Figure 6 IT5 mezzanine connector

The width of the ground cutouts, W_{GC}, is increased until the optimal impedance is met. Figure 8 shows the TDR impedance profiles of a couple of different cutout widths. It can be seen that increasing W_{GC} effectively increases the impedance of the overall capacitor impedance. Having a W_{GC} of 0.9mm yields an impedance that is slightly lower than the trace impedance. Since the capacitor geometry of Model 3 has shown to underestimate

the actual impedance by 1.2 ohms, a 0.9mm W_{GC} will actually give an impedance that closely matches the trace impedance.

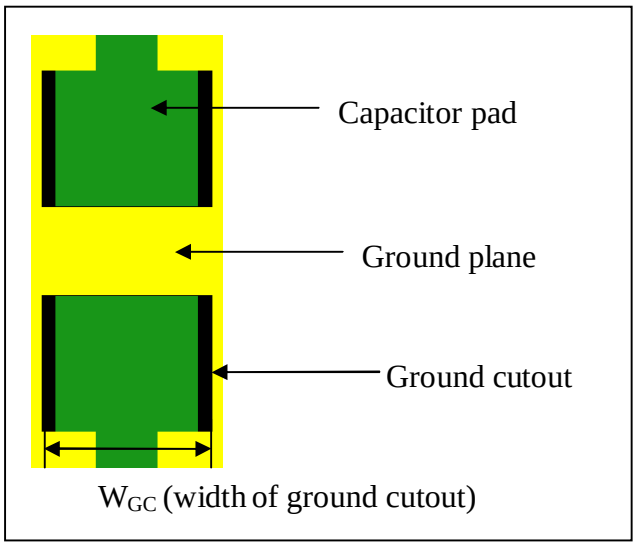


Figure 7 Capacitor footprint with ground cutout underneath capacitor pads

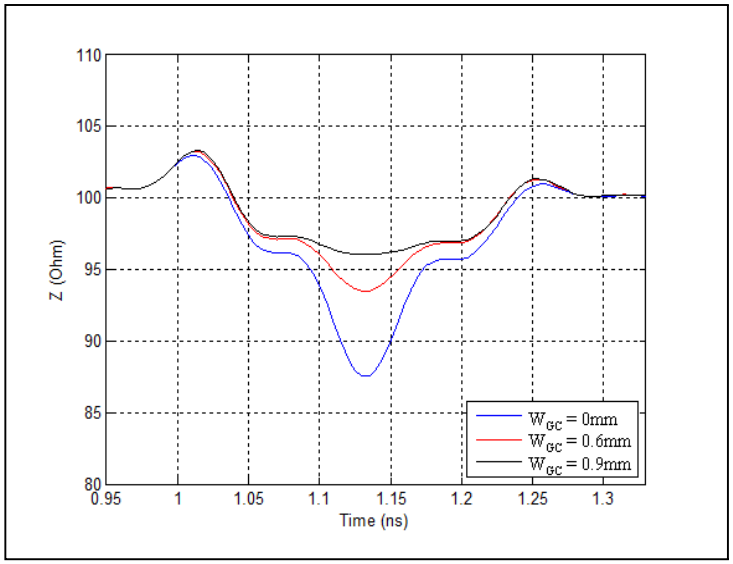


Figure 8 Simulated TDR impedance profile of capacitor with different ground cutout widths

In addition to impedance optimization, the capacitor placement is studied to minimize crosstalk. Two pairs of capacitors are modeled in HFSS, and two different arrangements are considered. In one arrangement, the two pairs of capacitors are placed in-line with each other. In the other arrangement, the two pairs are staggered from one another. These two arrangements are shown in Figure 9. Figure 10 shows the differential far end crosstalk (FEXT) of the two arrangements. It can be seen that the staggered arrangement has less crosstalk than the in-line arrangement. A similar staggered arrangement is used for the final wafer design.

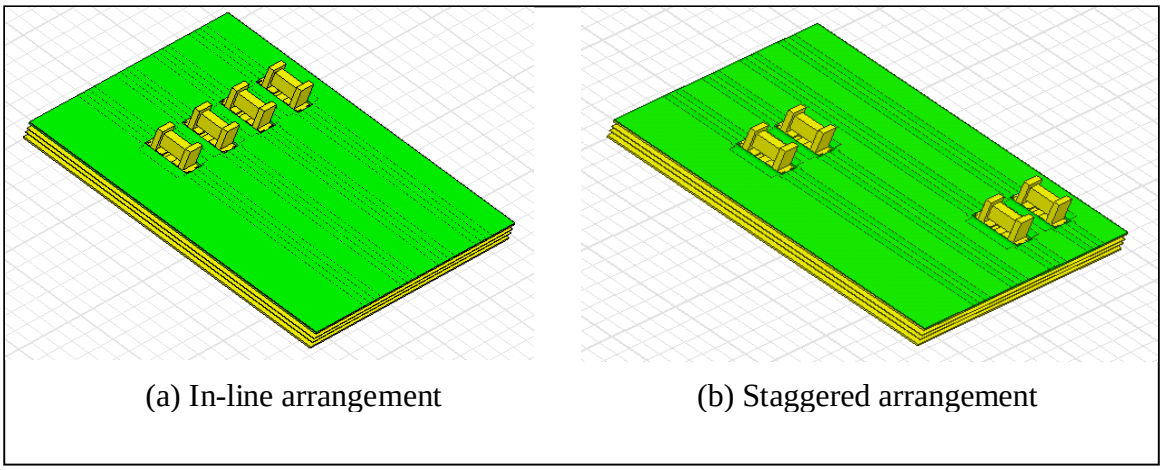


Figure 9 Capacitor arrangements for the study and minimization of crosstalk

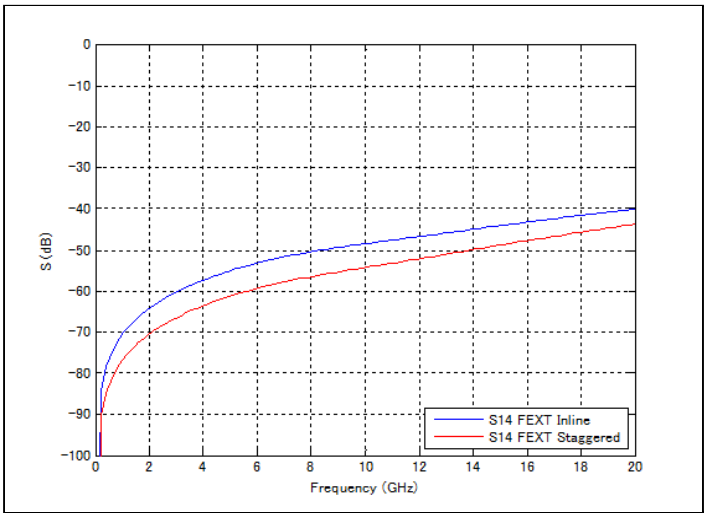


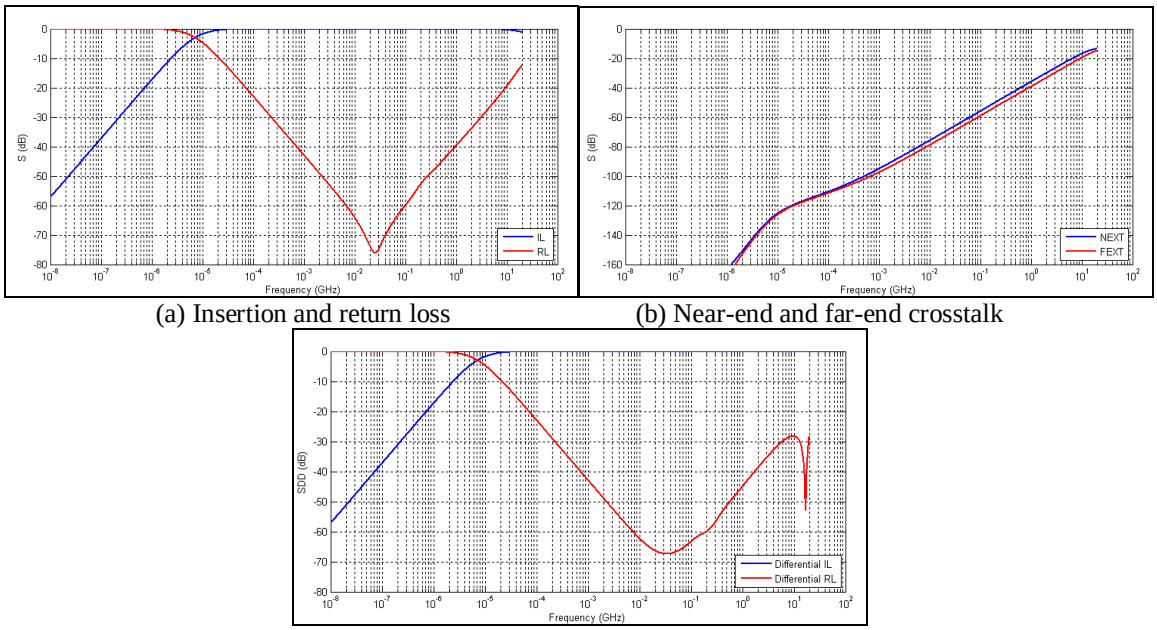
Figure 10 Differential FEXT of in-line arrangement (blue) and staggered arrangement (red) simulations

Low frequency modeling of capacitor

Though the metal block (Model 3) of Figure 4 mimics a capacitor's electrical behavior at high frequencies, it does not model the capacitor at DC or low frequencies. Our initial HFSS model starts at 200 MHz. To fill in the data below 200 MHz, we equate the S-parameters at 200 MHz to coupled transmission lines [1, 3] and cascade each transmission line with a 0.22 μF capacitor. The result is a complete DC blocking capacitor model that is valid from DC to 20+ GHz. Figure 11 shows the simulated insertion loss (IL), return loss (RL), near-end crosstalk (NEXT), far-end crosstalk (FEXT), and differential IL and RL of the capacitor pair in Figure 9.

It has been found that the capacitor model needs to be accurate not only near DC, but also in the transition region to high frequencies. Figure 12 shows the differential insertion and return losses in three different cases: Case 1 has a sufficient number of data points, Case 2 has missing data between 2MHz and 200 MHz, and Case 3 has missing data between 1

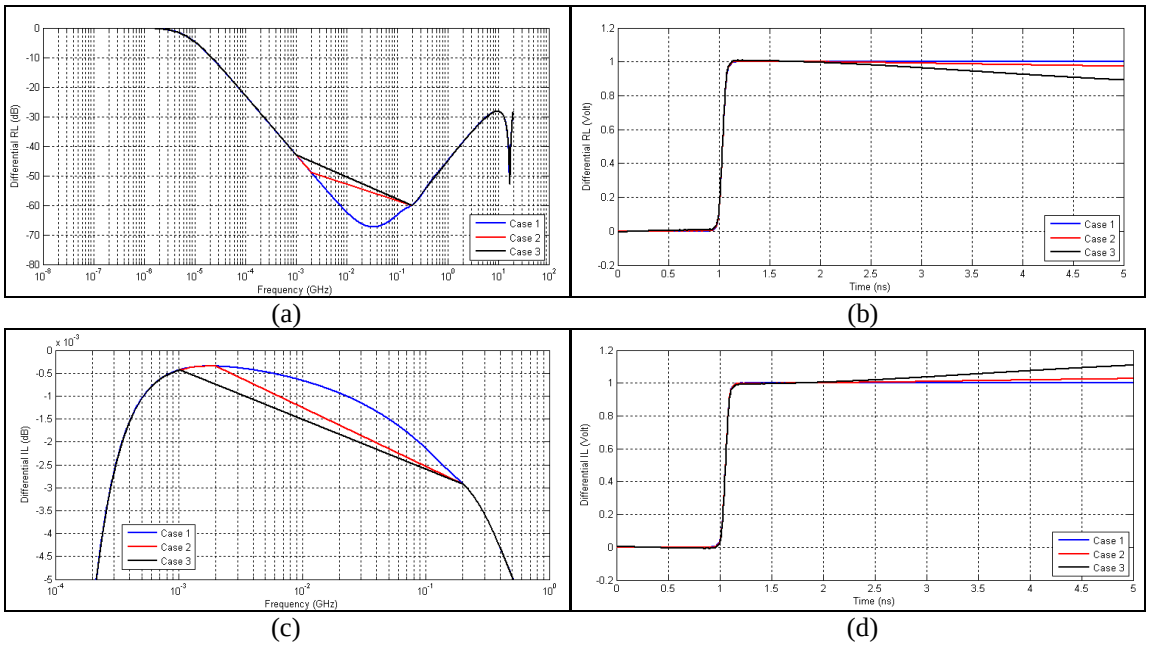
MHz and 200 MHz. Using IFFT to convert S-parameters to TDT waveforms at 50 ps (20% to 80%) rise time reveals something interesting: both Case 2 and Case 3 give rise to incorrect steady-state values. Therefore, to ensure correct time domain results, the S-parameters of DC blocking capacitor must be specified with enough data points at low frequencies.



(a) Insertion and return loss (b) Near-end and far-end crosstalk

(c) Differential insertion and return loss

Figure 11 Capacitor model that is valid from DC to 20+ GHz.



(a) (b)

(c) (d)

Figure 12 Differential RL and IL, and their corresponding TDR/TDT waveforms, of models with and without missing data points in the transitional frequency range.

Capacitor-only impedance and crosstalk study

A test coupon is made to study the impedance and crosstalk of only the on-board capacitors. Two pairs of capacitors are placed side by side as they are in the test channel with on-board capacitors. The capacitor vias are not included in this test coupon. All traces are routed on the surface using microstrip lines. These microstrip lines are routed to 2.4mm connectors. All lines are matched in length. Pictures of the test coupon can be seen in Figure 13. In order to allow multiple cables to connect to the 2.4mm connectors simultaneously, the connectors must be spaced out by a certain distance. Spacing out the connectors causes the traces to increase in length. To remove the effects of the traces, AtaiTec's In-Situ De-embedding (ISD) [3] is used for de-embedding. ISD takes in a measurement of lines that are twice the length of the lead-in traces to the DUT and uses them to de-embed out the impedance and crosstalk of the lead-in traces. It optimizes the insertion loss, impedance and crosstalk of the de-embedding traces to match the lead-in traces. Figure 14 shows an example of the impedance profile of the de-embedding trace, which matches the impedance of the lead-in trace. The extracted capacitor's IL, RL, NEXT, FEXT, and TDR impedance are all seen in good agreement with simulation (Figure 15 and Figure 16).

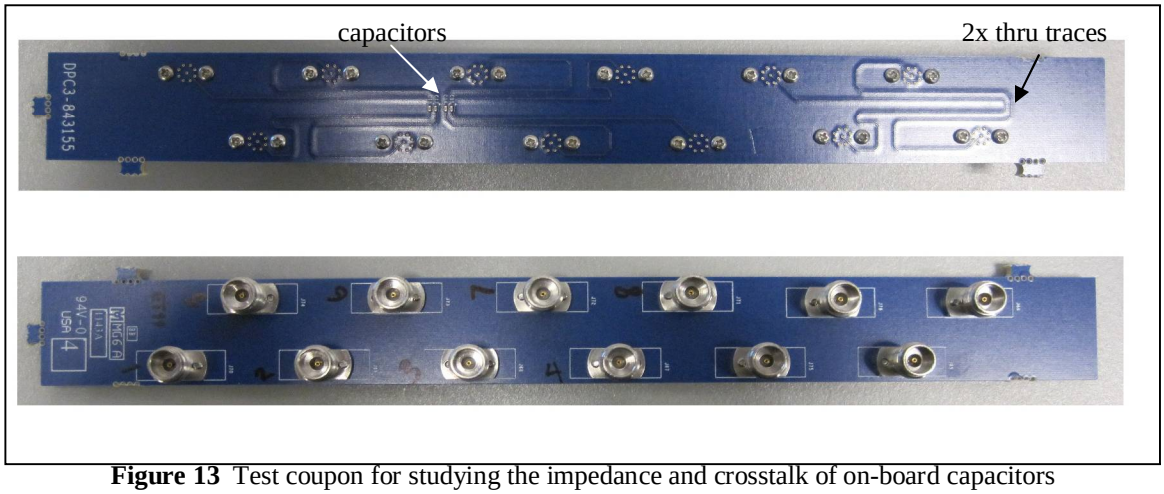
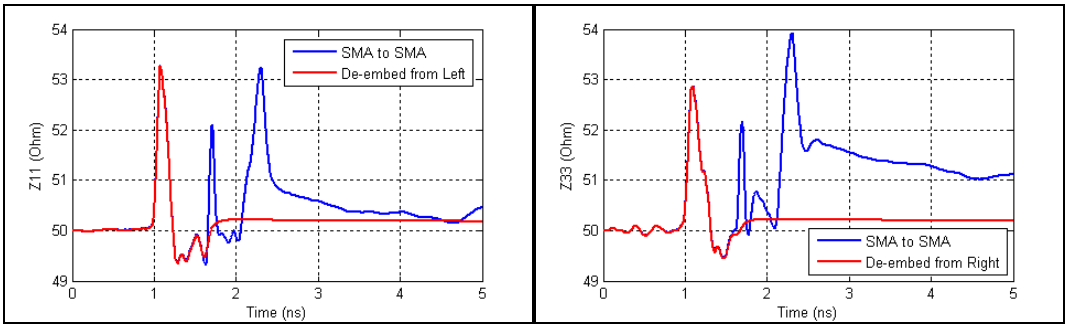


Figure 13 Test coupon for studying the impedance and crosstalk of on-board capacitors



(a) (b)

Figure 14 TDR impedance profile of capacitor test fixture measurement and de-embedding traces.

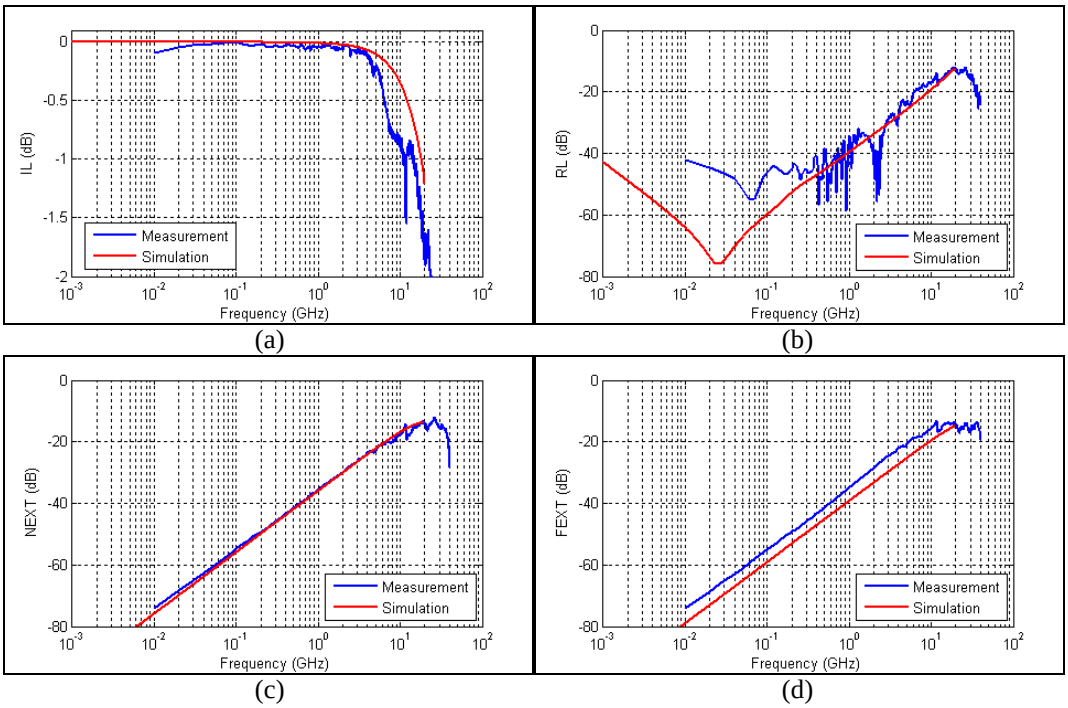


Figure 15 Measured vs. simulated IL, RL, NEXT, and FEXT comparison of a capacitor pair.

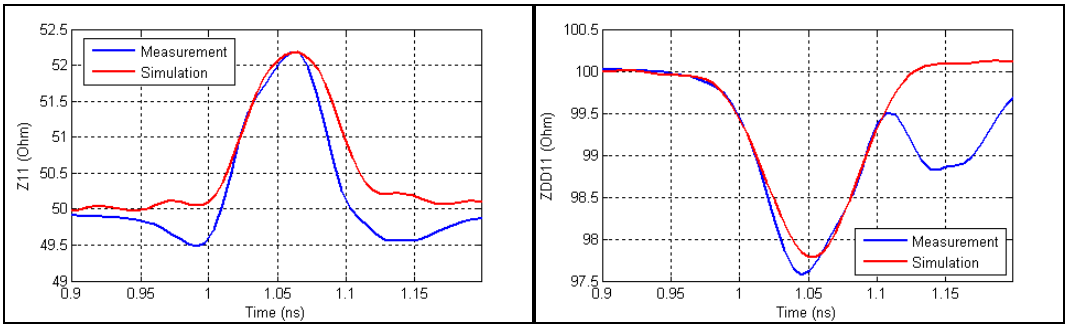


Figure 16 Measured vs. simulated single-ended and differential TDR impedance comparison of a capacitor pair at 50 ps (20% to 80%) rise time.

Full channel models

In order to study the impact that a connector with embedded DC blocking capacitors has on board design and channel performance, a couple of test channels are modeled and compared. One channel is meant to mimic a channel with capacitors on board and a connector without embedded capacitors. An illustration of this channel can be seen in Figure 17(a). It consists of the following.

1. 2.4mm connector with backdrilled via
2. Stripline trace
3. DC blocking capacitor with via
4. IT5 mezzanine connector (without embedded capacitors) with backdrilled vias

The other test channel is meant to mimic a channel with capacitors embedded into a

connector. This channel is illustrated in Figure 17(b) and it consists of the following.

1. 2.4mm connector with backdrilled via
2. Stripline trace
5. IT5 mezzanine connector with embedded capacitors and backdrilled vias

The board stackup consists of 30 metal layers with a total thickness of 120 mil. Megtron 6 material is used for the signal layers, and 370HR is used for other layers when possible. The stripline traces are routed through the middle layers. In both channels, there is a total of 12 inches of PCB trace. All vias are backdrilled with a maximum stub length of 12 mil. Four differential pairs are included in order to study crosstalk. In the IT5 connector, the nearest surrounding aggressors are studied: adjacent same wafer pair, adjacent different wafer pair, and diagonal pair. An illustration of these pairs can be seen in Figure 18. All surrounding unused signal pins are terminated with 50 ohm resistors. Since IT5 has a periodic structure, these 3 aggressors are representative of all 8 nearest surrounding aggressors.

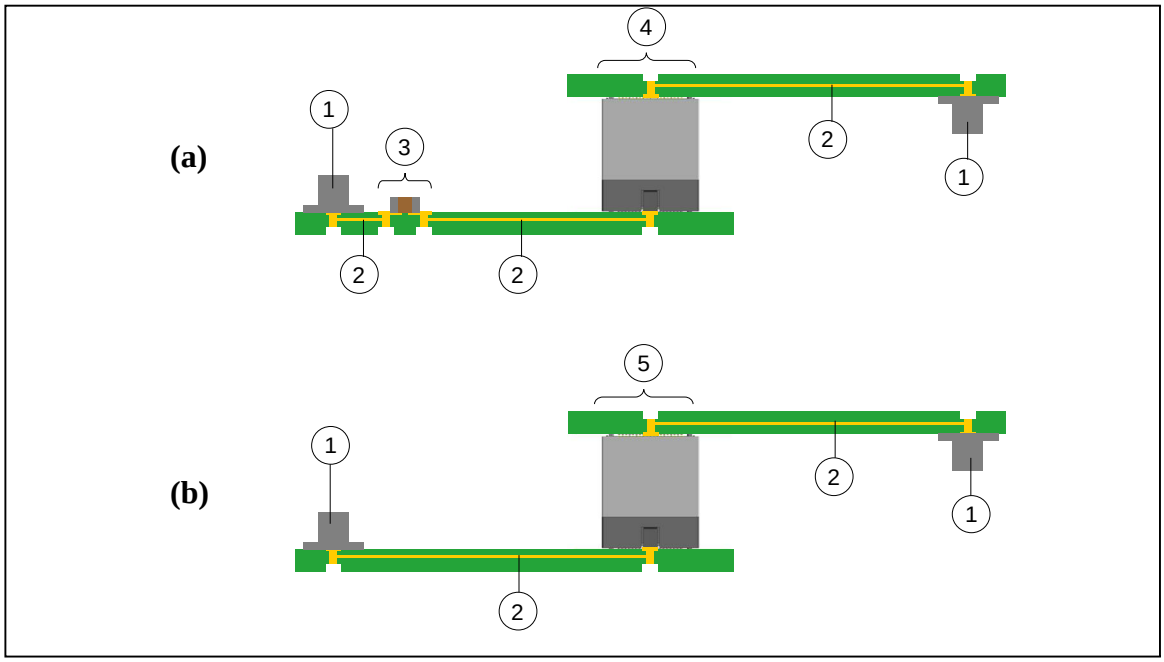


Figure 17 Test channels with (a) DC blocking capacitors on board and (b) DC blocking capacitors embedded in IT5

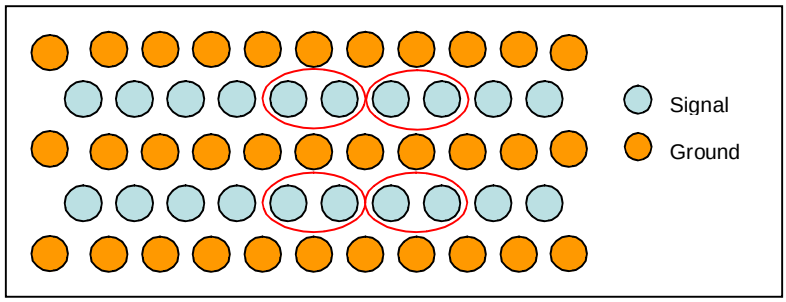


Figure 18 Differential pairs of IT5 studied in test channels

For the channel with capacitors on board, the capacitors are placed as close to each other as possible without violating fab rules or cutting off x or y direction routing. The placement and routing of the on-board capacitors can be seen in Figure 19. With such a placement and routing scheme, these four pairs of capacitors consume an area of 340mil by 160mil (8.6mm by 4.1mm). These may not seem like huge numbers, but in a very densely populated board with hundreds of capacitors, the area consumed by capacitors alone can be significant. Further, the routing underneath these capacitors becomes limited as the signal and ground vias of the capacitors pass through all layers of the board. By placing the capacitors inside of the connector, the board space can be utilized for other components and routing.

The components of the channels listed above are modeled separately. The 2.4mm connector, DC blocking capacitors, IT5, and their associated vias are modeled in HFSS. The stripline traces are modeled empirically to account for additional loss from surface roughness.

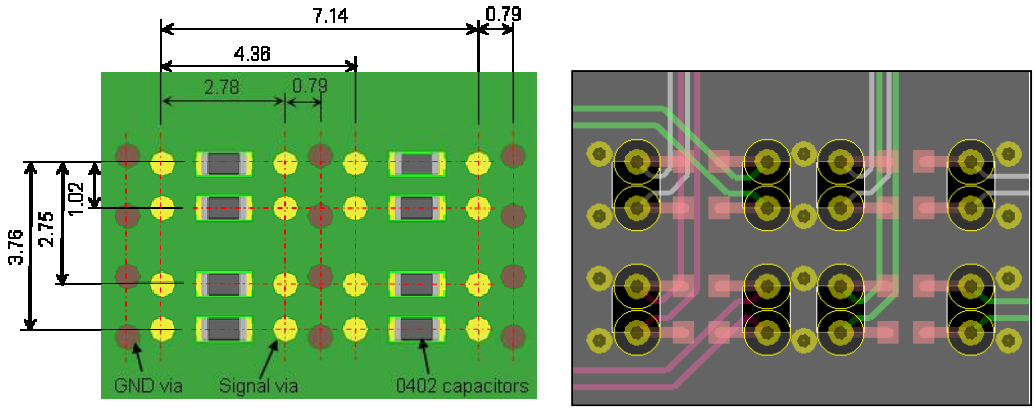


Figure 19 On-board capacitor placement and routing (dimensions in mm)

The on-board DC blocking capacitor footprints are optimized in a similar fashion as the embedded DC blocking capacitors. The capacitor vias are not considered in this optimization, as the vias would complicate the analysis. To speed up simulation time, the traces are shortened and wave ports are used instead of lumped ports. This reduces the simulation time by ¾. As a starting point, the 0.9mm wide cutouts underneath the capacitor pads are simulated. In this case, the pitch of the capacitors is narrower than the embedded capacitors. As a result, the coupling from capacitor to capacitor is larger, making the differential impedance lower. To increase the impedance, the cutout size is increased. Figure 20 shows some cutouts that are studied, and Figure 21 shows their simulated TDR impedance profiles. It can be seen that enlarging the cutouts from 0.9mm wide under the entire length of the capacitor footprint to a continuous 2mm wide cutout under the entire area only increases impedance by 0.5 ohms. Further increasing the cutout size would yield diminishing returns on impedance and may increase inter pair coupling. Therefore, the 2mm wide cutout is used for the test channel.

The four pairs of capacitors along with vias and some short traces are included in the capacitor model and simulated. To determine whether backdrilling the capacitor vias is necessary or not, two cases are simulated: without backdrilling and with backdrilling.

Figure 22 shows the differential insertion loss of the two cases. For 12.5Gbps, up to 6.25GHz, there is not much difference between the two. But if one were to design for 25Gbps, it can be seen that there is quite a bit of degradation caused by the via stubs beyond about 7GHz. For this test channel, capacitor vias with backdrilling are used.

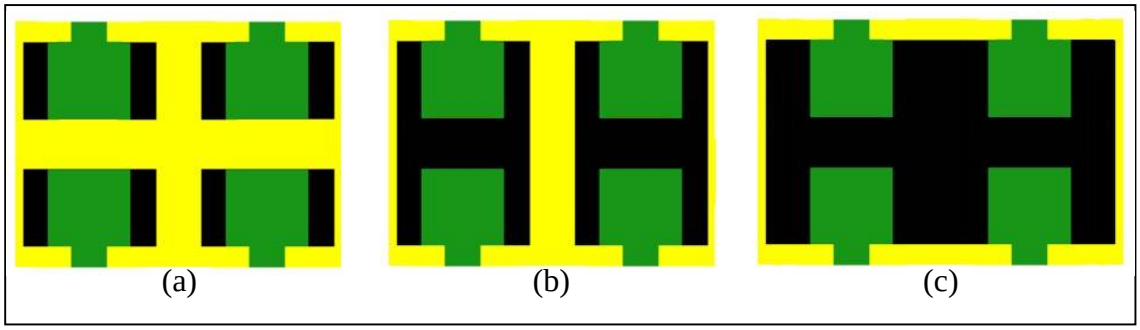


Figure 20 Cutouts studied for optimization of on-board capacitors (a) 0.9mm wide under capacitor pads, (b) 0.9mm wide under entire length of capacitor footprint, (c) 2mm wide under entire area

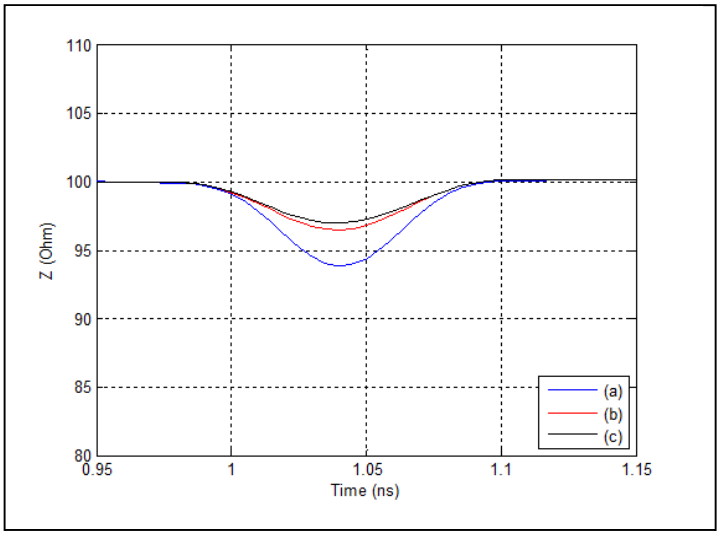


Figure 21 Simulated TDR impedance profiles of on-board capacitors with various cutouts (a) 0.9mm wide under capacitor pads, (b) 0.9mm wide under entire length of capacitor footprint, (c) 2mm wide under entire area

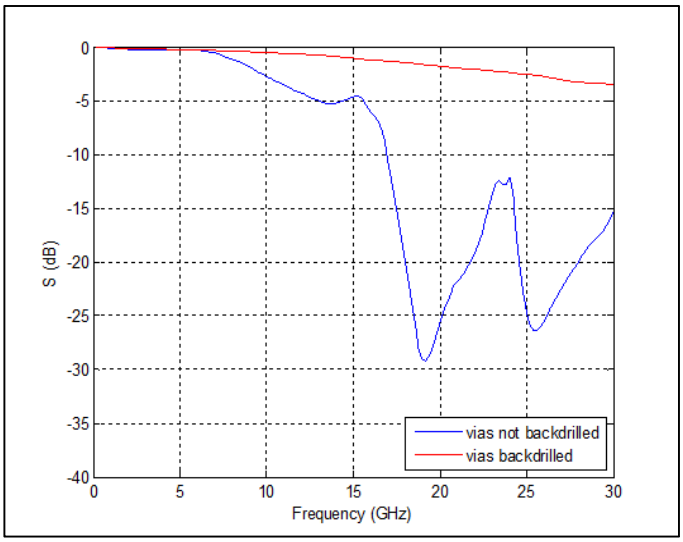


Figure 22 Differential insertion loss of capacitor models

To model the stripline traces, an empirical approach is taken. A test coupon is fabricated with a 12 inch trace and an 8 inch trace. Each trace consists of a 2.4mm connector, via, trace, via, and 2.4mm connector. The two traces are measured using Anritsu's VectorStar VNA. To remove the effects of the 2.4mm connectors and vias, Ataitec's In-Situ De-embedding (ISD)[4] is used. What remains are the extracted S-parameters of a 4 inch stripline trace. The single-ended insertion loss can be seen in Figure 23(blue). If a W-element model is extracted from a 2D field solver, the loss would be significantly underestimated, see Figure 23(red). According to Koul et al [5], the additional loss is due to a higher than specified dielectric loss tangent and copper surface roughness. The dielectric loss and rough conductor loss can be extracted with test coupons with various roughness profiles. The rough conductor loss can be fitted with

$$\alpha_r = b\sqrt{\omega} + c\omega + d\omega^2 \quad (1).$$

The dielectric loss can be fitted with

$$\alpha_D = e\omega + f\omega^2 \qquad (2).$$

However, we found that we could get a pretty good fit in this case if we drop $d\omega^2$, using

$$\alpha_r = b\sqrt{\omega} + c\omega \qquad (3),$$

and keeping the loss tangent fixed. The insertion loss with the fitted rough conductor loss can be seen in Figure 23(black).

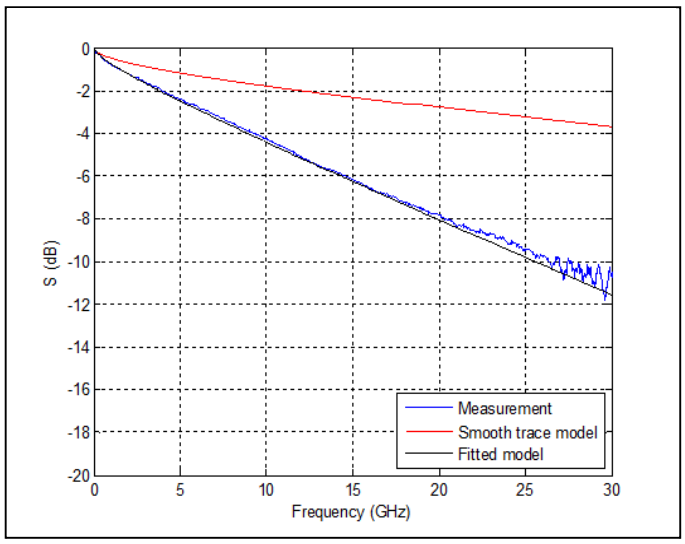


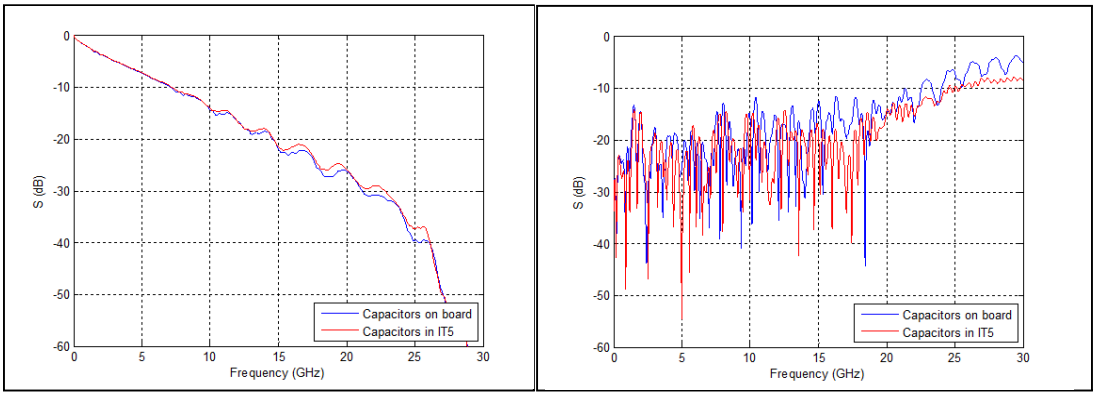
Figure 23 Single-ended insertion loss of 4 inches of stripline trace: measurement (blue), W-element (red), and model with conductor roughness fitted to measurement (black)

Full channel simulation results

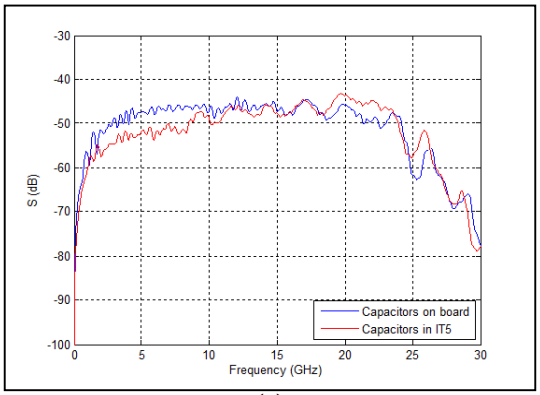
Figure 24 shows a comparison of the S-parameters of the two channels described above. It can be seen in Figure 24(a) that the differential insertion loss can be slightly improved if the DC blocking capacitors are placed inside of the connector rather than placed on board. This improvement in insertion loss is related to the slight improvement in differential return loss, shown in Figure 24(b). Because the capacitors are in the connector, capacitor vias are no longer needed on the board, eliminating the impedance discontinuities they cause. This effectively reduces return loss and improves insertion loss. Figure 24(c) shows the power sum of differential FEXT of the three surrounding aggressors mentioned above. The elimination of on-board capacitors and vias not only reduces return loss, it reduces FEXT as well. Such a reduction can be seen up to about 15GHz.

The above improvements are reflected in the insertion loss to crosstalk ratio (ICR) with respect to FEXT, shown in Figure 25. The ICR curves of the two channels are plotted along with the IEEE 802.3ap ICR specification, which is kept constant here beyond 5.15625GHz. Placing capacitors inside of the connector increases the margin.

Agilent's Advanced Design System (ADS) statistical simulations are run on the two channels to see what difference the connector with embedded DC blocking capacitors would make on the eye diagram. The channels are simulated at two data rates, 12.5Gbps and 25Gbps. A $1V_{P-P}$ input voltage is used. Feed forward equalization (FFE) is applied with 1 pre and 2 post cursors. No receiver equalization is used. The touchstone files of the above models are used with the three FEXT aggressors. The resulting eye diagrams of the channel with capacitors embedded in IT5 are shown in Figure 26. Table 1 shows the eye heights and widths of the eye diagrams at bit error rate (BER) of 10E-15. Having the capacitors inside of IT5 rather than on the board does indeed increase the eye opening at 12.5Gbps and at 25Gbps, even with the on-board capacitors and vias being optimized.



(a) (b)



(c)

Figure 24 S-parameters of channel model with capacitors on board (blue) and channel model with capacitors in IT5 (red): (a) Insertion loss, (b) return loss, and (c) power sum of FEXT

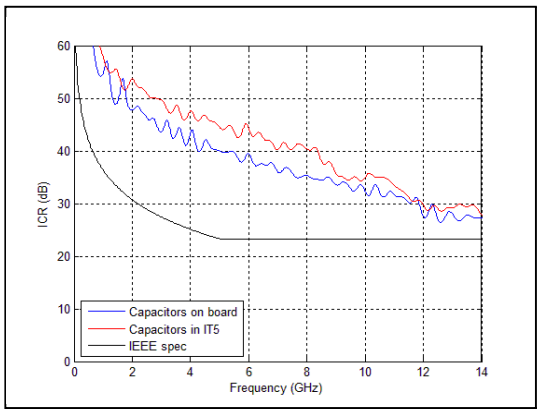


Figure 25 ICR with respect to FEXT of channel model with capacitor on board (blue) and channel model with capacitors in IT5 (red)

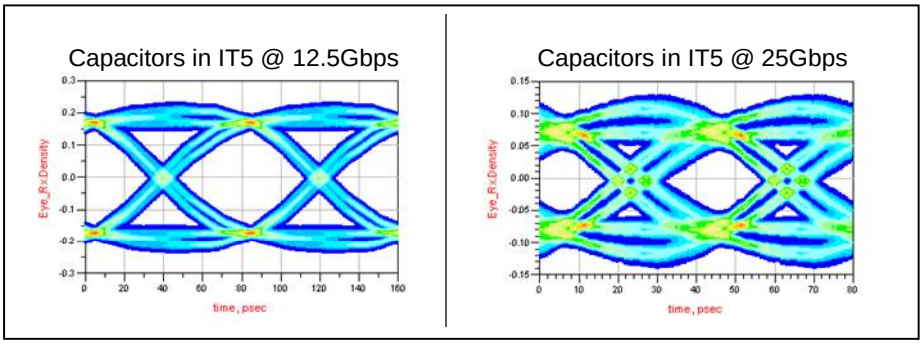


Figure 26 Channel simulation eye diagrams of channel model with capacitors in IT5 at 12.5Gbps and 25Gbps

Table 1 Eye heights and widths at BER 10E-15

	12.5Gbps		25Gbps	
	Height (mV)	Width (UI)	Height (mV)	Width (UI)
Capacitors on board	275	0.785	91	0.585
Capacitors in IT5	289	0.795	92	0.615

Full channel measurement results

To validate the channel models, a test fixture of the two test channels is fabricated, assembled, and measured. The fully assembled test fixture is shown in Figure 27. The fixture includes the two channels described above: channel with DC blocking capacitors on board and channel with DC blocking capacitors in IT5. Measurements of the fixture are taken with Anritsu's VectorStar VNA. The S-parameters are converted to a TDR impedance profile using ADK and can be seen in Figure 28. Although the capacitor vias are backdrilled, they still leave some impedance discontinuities in the channel. These discontinuities are not present in the channel with capacitors in IT5.

Figure 29 shows the measured S-parameters of the test channels. Just as the simulation model predicts, the channel with capacitors in IT5 gives a slight improvement to the insertion loss and return loss and reduces FEXT. Measurement also verifies that a connector with embedded DC blocking capacitors can significantly improve the ICR, which is shown in Figure 30.

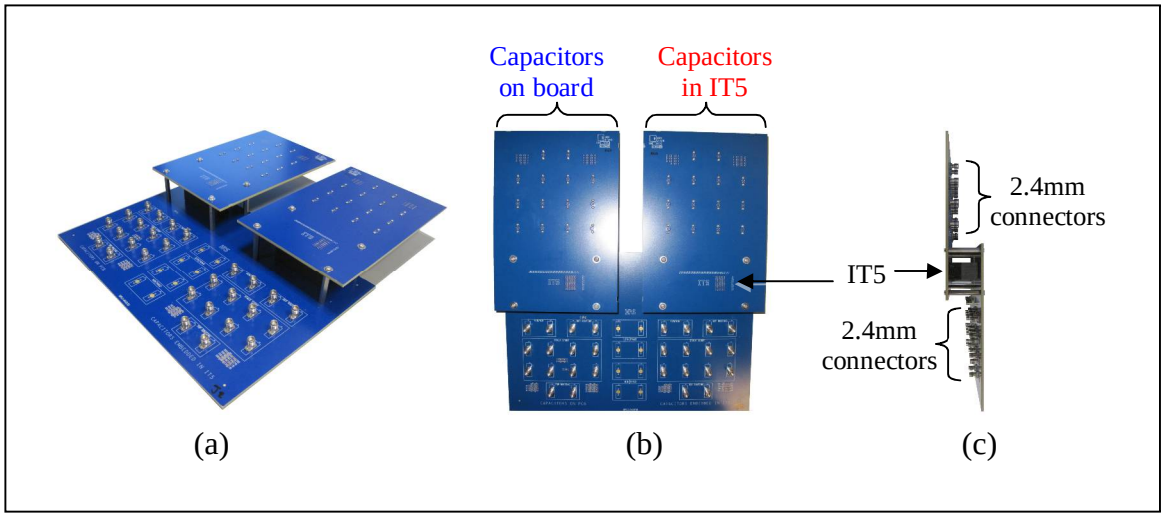


Figure 27 Test fixture of full channels: (a) perspective view, (b) top view, (c) side view

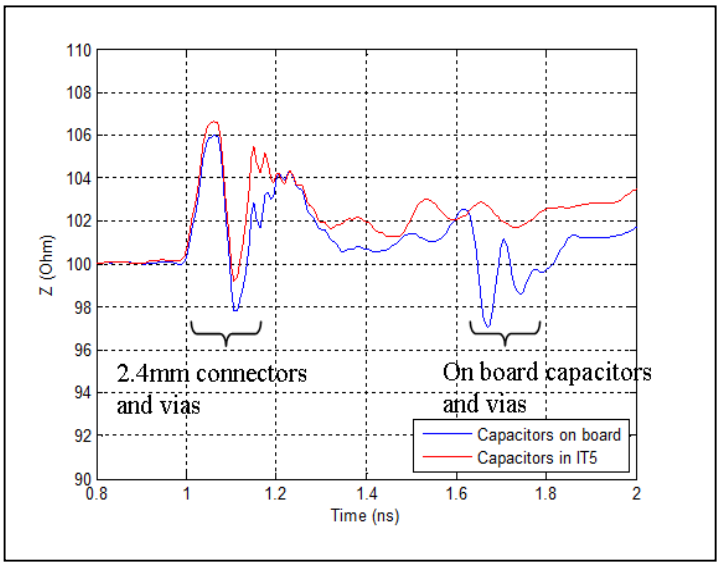


Figure 28 Measured TDR impedance profile (30ps 20-80% rise time) of channel with capacitors on board (blue) and channel with capacitors in IT5 (red)

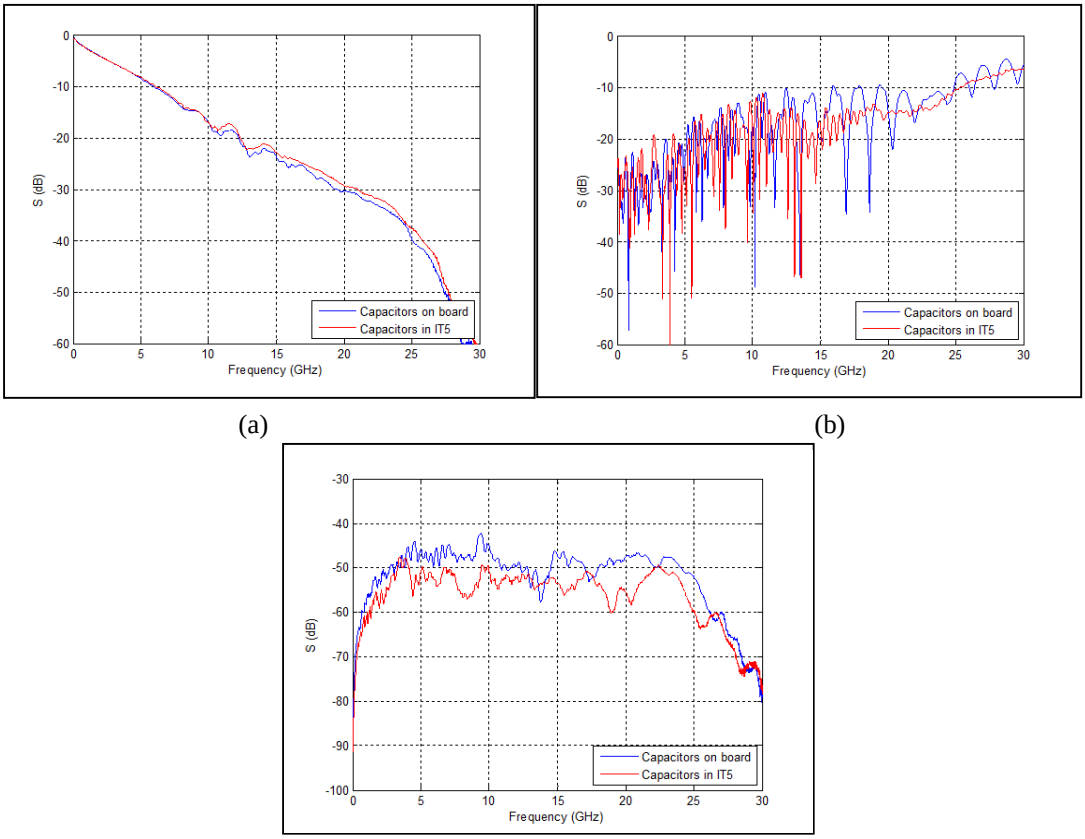


Figure 29 Measured S-parameters of channel with capacitors on board (blue) and channel with capacitors in IT5 (red): (a) insertion loss, (b) return loss, and (c) power sum of FEXT

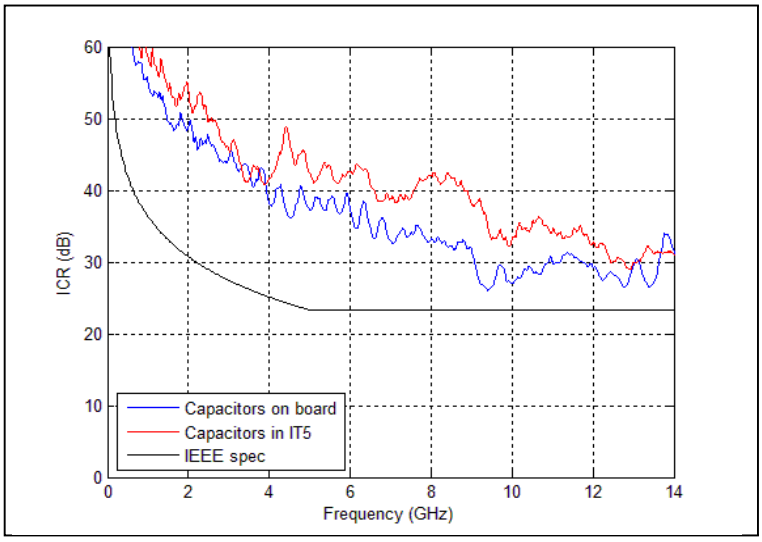


Figure 30 Measured ICR with respect to FEXT of channel with capacitors on board (blue) and channel with capacitors in IT5 (red)

Summary

This work presented a solution to increase board and routing space by removing DC blocking capacitors from the board and embedding them into a high speed, high density connector. The effects of this solution on Signal Integrity performance in a multi-gigabit chip-to-chip serial link were studied. A channel with on-board DC blocking capacitors and a channel with DC blocking capacitors embedded in IT5 were modeled, fabricated, and measured. It was seen from the channel models that placing the capacitors in IT5 improved the insertion and return losses of the channel and decreased crosstalk. Measurements were taken on the fabricated channels, and the results are in good agreement with simulation. This solution effectively increases board and routing space and improves Signal Integrity performance of the channel. In addition to studying channel performance, a couple of useful methods of modeling and characterizing capacitors and PCB traces were presented.

References

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2. Takashi Kikuchi, Gnyaneshwar Ramakrishna, Quyen Chu, Hien Ly, Sundar Sethuraman, Chrys Shea, Jean-Paul Clesh, "Long-term Reliability Assessment of a New Lead-Free Area Array Connector System," South East Asia Technical Conference on Electronics Assembly Technologies by SMTA Penang, 2011.
3. Ching-Chao Huang, "Signal integrity modeling and simulation tools," DesignCon 2004.
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5. Amendra Koul, Marina Y. Koledintseva, Scott Hinaga, and James L. Drewniak, "Differential extrapolation method for separating dielectric and rough conductor losses in printed circuit boards," IEEE Trans. Electromagnetic Compatibility, 2011.