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Hacking Skew Measurement

Clement Luk, Hirose Electric
cluk@hirose.com

Jeremy Buan, Hirose Electric
jbuan@hirose.com

Tadashi Ohshida, Hirose Electric
tohshida@hirose.com

Pin Jen Wang, Hirose Electric
pwang@hirose.com

Yuta Oryu, Hirose Electric
yoryu@hirose.com

Ching-Chao Huang, AtaiTec Corporation
huang@ataitec.com

Neil Jarvis, Rohde & Schwarz
Neil.Jarvis@rsa.rohde-schwarz.com

Abstract

For high-speed and EMC applications, it is crucial, but difficult to quantify the signal path skew of device under test (DUT). When the device is mounted on a PCB fixture, the PCB trace skew adds extra uncertainty to the measurement data. Attempting to de-embed such PCB trace skew by separate test coupons just introduces even more error if the test coupons have opposite skew. Besides showing how de-embedded results can vary, depending on the skew of test coupons and/or fixture, this paper introduces a new methodology, dubbed In-Fixture Skew Subtraction (IFSS) method, to quantify DUT skew without de-embedding. A simple equation has been derived to compute both PCB and DUT skews for those cases where the DUT has distinguishable impedance discontinuities.

Authors Biography

Clement Luk is a Senior Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. He is involved in high speed connector design, device and channel simulation and measurement. He received his BSCS and MSEE from University of Wisconsin-Madison.

Jeremy Buan is a Signal Integrity Manager in the High-Speed Interconnect section at Hirose Electric USA, Inc. As an SI Manager, he supports the development of high-speed connectors by both simulation and measurement. He gives SI/design assistance to customers by providing connector models, evaluation boards, channel simulation data and via breakout optimization. Jeremy received his BSEE and MSEE from San Jose State University.

Tadashi Ohshida is an Engineering Manager in the High-Speed Interconnect section at Hirose Electric USA, Inc. He joined Hirose in 2001 as a connector development engineer for computer and telecom market. He received his BSEE from Iwate University, Iwate, Japan.

Pin Jen Wang (Alvin) is a Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. He is working on connector model simulation, measurement, correlation, and development, characterization board design, and PCB material characterization. He received his BSEE and MSEE from University of Idaho.

Yuta Oryu is a Signal Integrity Engineer at Hirose Electric USA in the High-Speed Interconnect Department. He received his BSEE from University of Rochester.

Ching-Chao Huang, founder and president of AtaiTec Corporation, has more than 30 years of high-speed design and SI software development experience. He was advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member and he pioneered In-Situ De-embedding (ISD) for

causal and accurate de-embedding. He received his BSEE from National Taiwan University and MSEE and PhD from Ohio State University.

Neil Jarvis is an Applications Engineer at Rohde and Schwarz USA, Inc. He has over 25 years of experience in RF, Microwaves, and Vector Network Analysis. He currently supports VNA signal integrity applications including USB, HDMI, PCIE, and SATA. Neil has a BSEE from San Jose State University, an MS from The Naval Postgraduate School in Systems Analysis, and an MBA from Pepperdine University.

Introduction

Many of today's high-speed serial data standards use differential signaling to reduce noise and EM emission. One of the challenges is the requirement that the p- and n-transmission paths be of equal electrical delay. When these paths are not equal in delay, skew arises. Skew increases differential insertion loss and EMC emission. As a result, skew can limit a system's bandwidth, add data-dependent jitter, and reduce ability to equalize a channel.

Skew and differential insertion loss are among the most important criteria for high-speed system designers. PCB and component manufacturers need to provide those information accurately for their products. De-embedding has been used routinely to characterize the electrical performance of device under test (DUT). When the device is mounted on a PCB fixture (or when the device is part of PCB itself), the PCB trace skew adds extra uncertainty to the measurement data. Attempting to de-embed such PCB trace skew by separate test coupons just introduces even more error if the test coupons have opposite skew. Error in the DUT skew after de-embedding can lead to misinterpretation of other de-embedded DUT results. For example, PCB manufacturers may mistakenly conclude their differential trace attenuation is too high when in fact the data were tainted with skew error.

This paper uses actual PCB trace measurement data to demonstrate how de-embedded results can vary, depending on the skew of reference coupons and/or fixture. Without knowing actual fixture skew, we face the dilemma of whether we should include the coupon's skew in de-embedding. The de-embedded trace attenuation, with or without including the coupon skew, is compared with eigenvalue solution. (The eigenvalue solution operates on differential data only and has no skew information.)

To pave the way for de-embedding correct fixture skew, this paper introduces a new methodology, dubbed In-Fixture Skew Subtraction (IFSS), to quantify fixture and DUT skew before de-embedding. A simple equation has been derived to compute both PCB and DUT skews for those cases where the DUT has distinguishable impedance discontinuities. A test vehicle, consisting of separately measurable PCB trace fixtures and DUT, was fabricated. Directly measured DUT skew and calculated skew using the proposed IFSS method are compared. To see if the proposed IFSS method is applicable to more complex devices, Hirose IT8 connector simulation model was studied. Results and key takeaways are summarized in the following sections.

What is DUT skew

The skew (i.e., delay difference between two signal paths) in connector, PCB trace and cable must be accurately characterized because it can have detrimental effect on high-speed differential signaling (for example, see Figure 5 of [1]). The device under test

(DUT) is often mounted on a PCB fixture for characterization. However, the fixture introduces additional ambiguity to the skew measurement.

Consider Figure 1 where p1, p2, p3 and n1, n2, n3 denote the p- and n- delay of the left-fixture, DUT and right-fixture, respectively. The total delay from Ports 1 to 2 and Ports 3 to 4 (i.e., p1+p2+p3 and n1+n2+n3) can be measured and the DUT skew (i.e., p2–n2) is to be found.

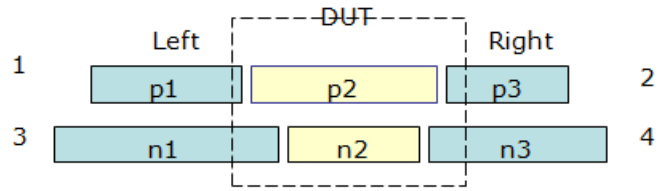

Figure 1. Delay of fixture + DUT.

De-embedding

De-embedding the fixture to characterize DUT usually requires a reference coupon. The simplest de-embedding method is with a "2x thru" reference coupon, which is subtracted either directly [2] or with impedance correction [3-4].

Consider Figure 2 where p4 and n4 denote the p- and n- delay of 2x thru. If the 2x through's skew is included directly for de-embedding, then

$$\begin{aligned}\text{De-embedded skew@DUT} &= (p1 + p2 + p3 - p4) - (n1 + n2 + n3 - n4) \\ &= (p2 - n2) + \big(p1 + p3 - (n1 + n3)\big) - (p4 - n4) \\ &= \text{Skew@DUT} + \text{Skew@Fixture} - \text{Skew@Coupon}\end{aligned}$$

Due to PCB fiber weave and manufacturing variation, there is no way to guarantee that Skew@Fixture and Skew@Coupon are identical. In fact, when Skew@Fixture and Skew@Coupon are of opposite sign, De-embedded skew@DUT can become worse than without using a reference coupon!

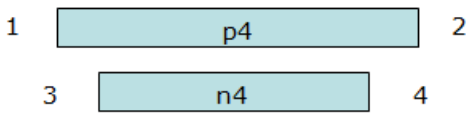

Figure 2. Delay of 2x thru.

Effect of skew on de-embedding

Figure 3 shows a measurement example of insertion loss and phase delay of 2" and 7" stripline differential structures where the frequency-dependent skew can be clearly seen. Time-domain skew can be calculated by converting single-ended insertion loss into TDT step response and measuring the delay at 50% of the settling voltage. Using 5ps rise time (20/80), we get the skew of –1.15843ps and 0.909807ps for the 2" and 7" structures, respectively.

Figure 4 shows the DUT (i.e., 5" trace-only) results after de-embedding the 2" structure from 7" structure. Two methods were used: including or ignoring the coupon (2" structure) skew [4]. In this case, including the coupon skew leads to more DUT skew because the coupon (2" structure) and fixture + DUT (7" structure) have skew of opposite sign. As shown in Figure 4, more DUT skew results in more differential insertion loss.

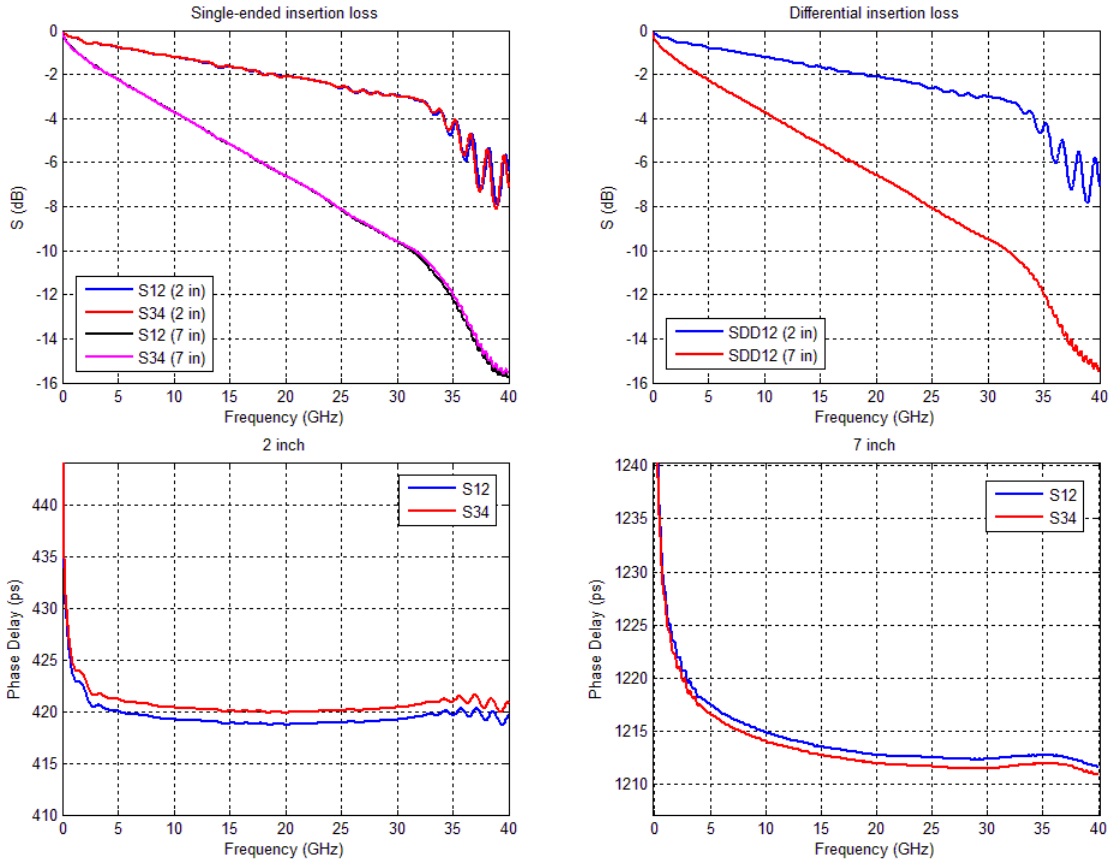

Figure 3. 2" and 7" stripline differential structures with opposite skew.

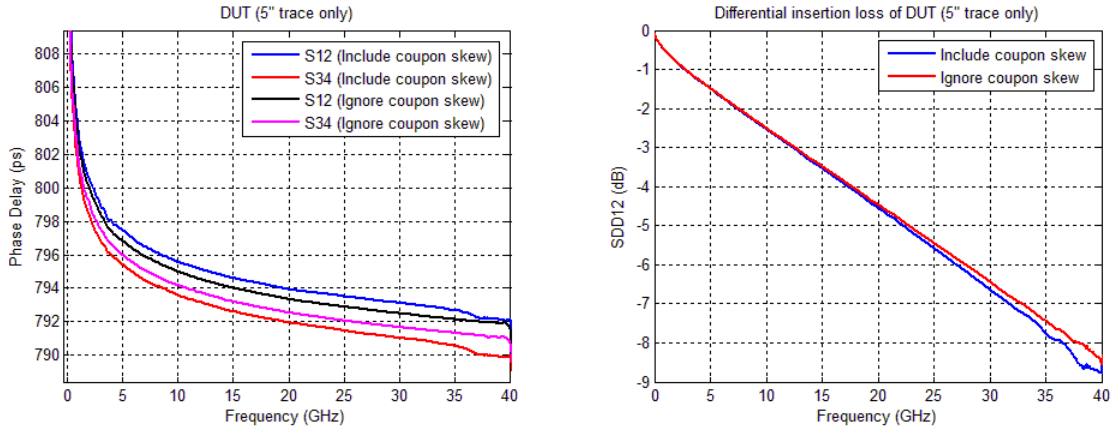

Figure 4. Single-ended phase delay and differential insertion loss of 5" PCB traces after de-embedding.

De-skew

It is important that skew does not contaminate the results when high-speed designers and PCB manufacturers talk about "loss per inch". Figure 5 shows the single-ended phase delay and differential insertion loss after de-skewing (by padding ideal transmission line to the shorter trace to match the phase delay of longer trace). The readings of differential insertion loss are now more consistent, whether or not skew is included during the de-embedding process. Some minute difference still exists, partially due to the difference in phase delay. In this case, including skew in de-embedding resulted in larger skew and therefore larger phase delay after de-skewing.

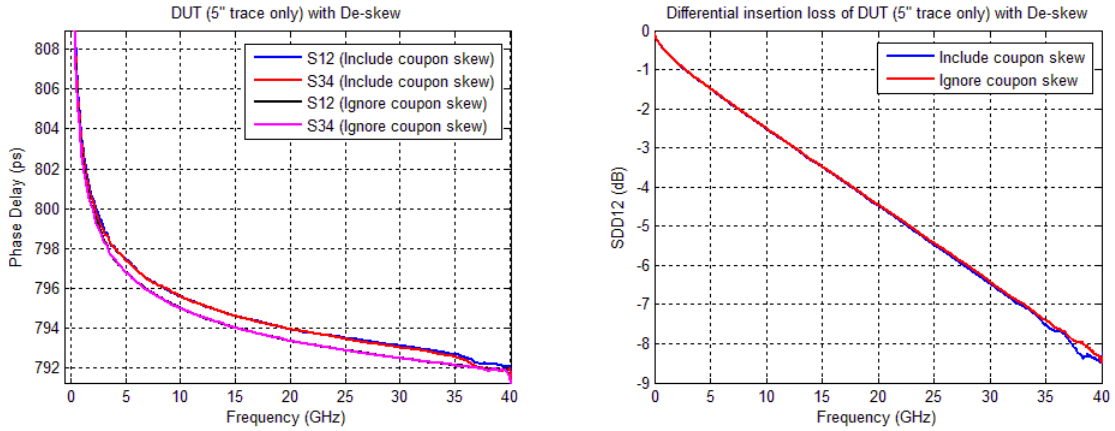

Figure 5. Single-ended phase delay and differential insertion loss of 5" PCB traces after de-skewing.

Eigenvalue solution

It is of interest to compare the de-embedded results with eigenvalue solution (see Page 14 of [5], for example). The eigenvalue solution operates on the differential (or common) mode directly so it has no information concerning DUT skew. Figure 6 compares the de-skewed results of Figure 5 with the eigenvalue solution. Glitches and spikes in the eigenvalue solution are seen, due in part to the difference between coupon and fixture, and in part to the assumption of uniform transmission line for DUT [5].

To compare with the eigenvalue solution more directly, we could also do de-embedding on differential mode only. Figure 7 compares the de-embedded results (using only differential data in ISD [4]) with eigenvalue solution. The results are now more similar to each other except that ISD does not give the same glitches or spikes as eigenvalue. This is because ISD does not assume identical coupon and fixture or uniform transmission line for DUT. To be accurate, differential DUT response should be obtained by de-embedding the fixture's 4-port S parameters instead of the differential 2-port S parameters. The effect of skew and mode conversion must be accounted for during the de-embedding process.

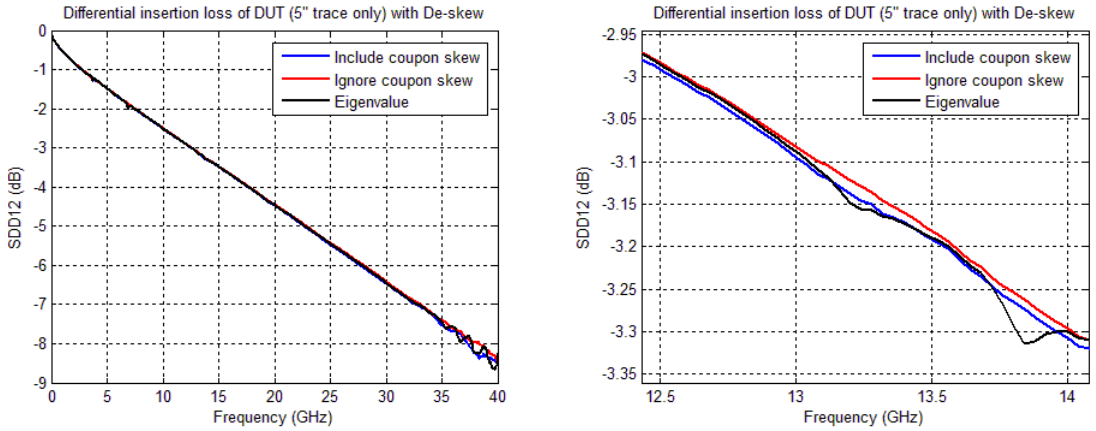

Figure 6. De-embedded SDD12 vs. attenuation calculated by eigenvalue.

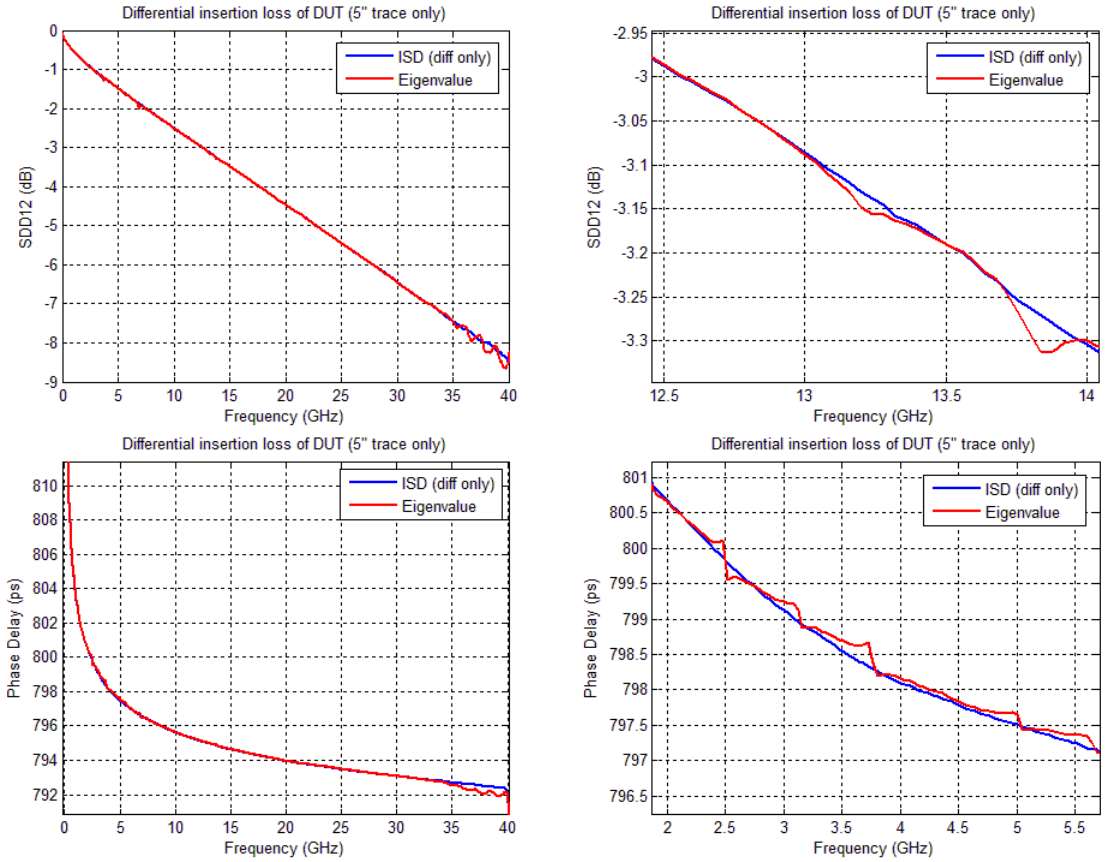

Figure 7. De-embedded SDD12 magnitude and phase delay (using only differential data in ISD [4]) vs. eigenvalue solution.

The question now is, should we or should we not include the coupon's skew for de-embedding. The skew and insertion loss of differential PCB traces are among the most important parameters to be characterized, but attempting to characterize them by de-embedding looks somewhat cloudy. The following section proposes a method to identify Skew@Coupon, Skew@Fixture and Skew@DUT beforehand. Such information will help improve the de-embedding accuracy of differential structures.

In-Fixture Skew Subtraction (IFSS)

This paper proposes a method, dubbed In-Fixture Skew Subtraction (IFSS), that derives the DUT skew without de-embedding. The requirement is that there exist impedance markers close to the entrance and exit of DUT. These impedance markers can be either local maxima or local minima, and can be part of the DUT or manually created discontinuities on PCB.

Derivation of DUT skew

Following Figure 1, let T1, T2 and T3 denote the total skew of fixture + DUT, left fixture + DUT and right fixture + DUT, respectively:

$$T1 = (p1 + p2 + p3) - (n1 + n2 + n3) = (p1 - n1) + (p2 - n2) + (p3 - n3)$$

$$T2 = (p1 + p2) - (n1 + n2) = (p1 - n1) + (p2 - n2)$$

$$T3 = (p3 + p2) - (n3 + n2) = (p3 - n3) + (p2 - n2)$$

Then,

$$\text{Skew@DUT} = p2 - n2 = T2 + T3 - T1$$

$$\text{Skew@Left} = p1 - n1 = T1 - T3$$

$$\text{Skew@Right} = p3 - n3 = T1 - T2$$

We will compute T1 from TDT of S12 and S34, T2 from TDR of S11 and S33 and T3 from TDR of S22 and S44, respectively.

Using the previous example of 7" stripline differential structure with 5ps rise time (20/80) and brickwall filter, we get T1=0.909807ps at 50% of settling voltage (see Figure 8).

The TDR waveforms looking into the left and right fixtures give T2=1.3525ps in Figure 9 and T3=0.904286ps in Figure 10, respectively. Note that a factor of 2 was accounted for when measuring the delay between two local minima (or maxima) of TDR waveforms. Then, the 7" trace-only skew is given by

$$\text{Skew@7" DUT} = T2 + T3 - T1 = 1.3525 + 0.904286 - 0.909807 = 1.346979ps$$

If the skew is uniformly distributed, then

$$\text{Skew@5" DUT} = 1.346979 \times \frac{5}{7} = 0.962128ps$$

Following similar procedures, we get T1=–1.15843ps, T2=–1.60738ps and T3=–1.47965ps for the 2" stripline structure. For comparison, de-embedding gives 2.068237ps (=0.909807+1.15843) and 0.909807ps for 5" DUT in this case, with or without including the 2" structure (coupon) skew.

The 2" trace-only skew is derived from the 2" structure as

$$\text{Skew@2" DUT} = T2 + T3 - T1 = -1.60738 - 1.47965 + 1.15843 = -1.9286ps$$

The statistics of per-inch trace-only skew is often of interest. We have now arrived at a range of –0.9643ps (=–1.9286/2) to 0.192426ps (=1.346979/7) from the above 2" and 7" structures without de-embedding.

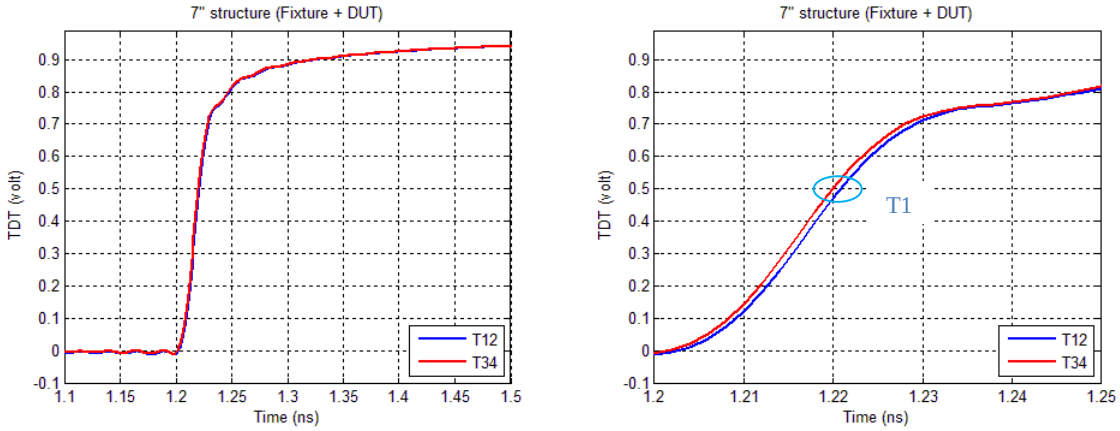

Figure 8. Computing total skew (T1) of fixture + DUT from TDT.

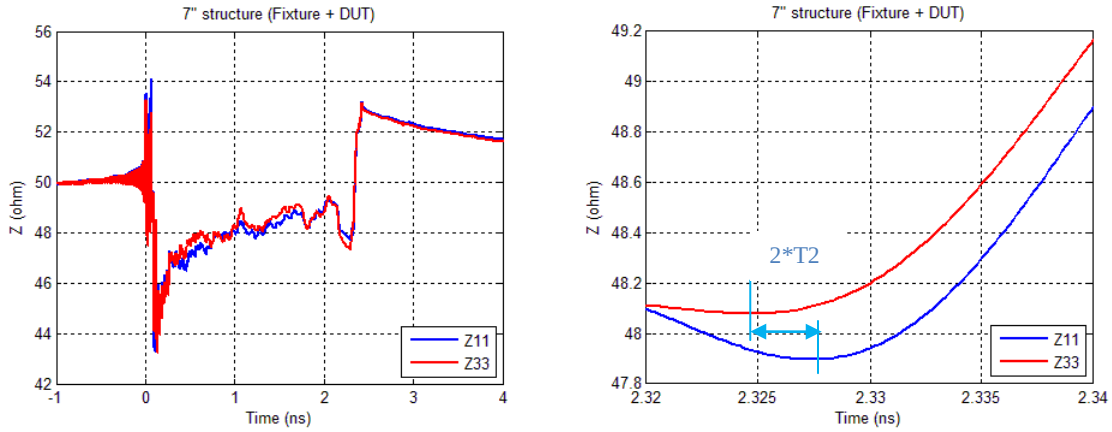

Figure 9. Computing total skew (T2) of left fixture + DUT from TDR.

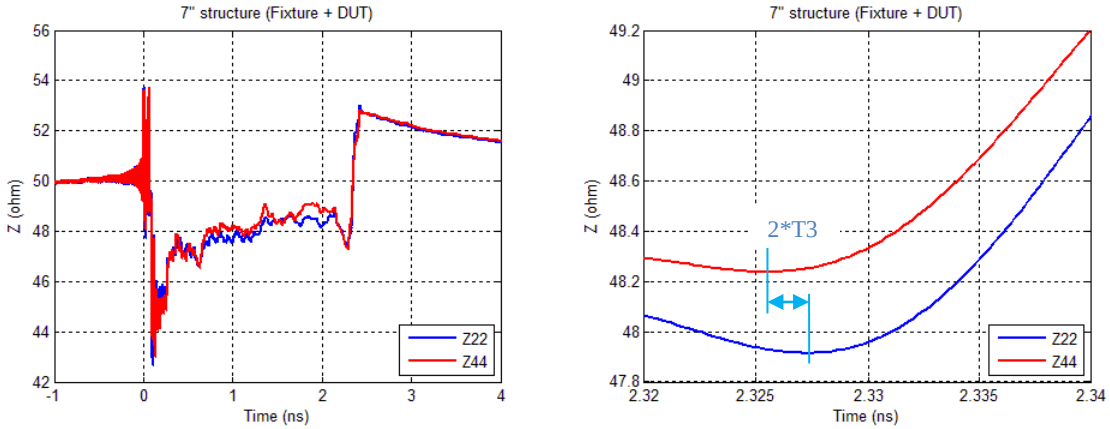

Figure 10. Computing total skew (T3) of right fixture + DUT from TDR.

Validation vehicle

To validate the proposed skew calculation method, we built a test vehicle inspired by the IEEE P370 plug-and-play board. The test vehicle consists of three separately measurable boards connected by male-to-male connectors (Figure 11). The three boards are (1) Left fixture board, (2) Right fixture board and (3) DUT board. The DUT itself is a coplanar waveguide with 100Ω differential impedance.

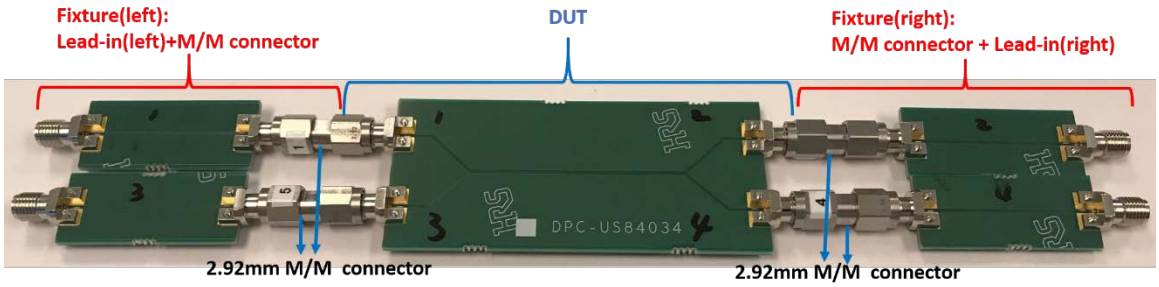

Figure 11. Left-fixture + DUT + right fixture boards.

Fixture and DUT board

The fixture and DUT boards are 4-layer FR408 boards of 57mil thickness. On the edges of each fixture and DUT board, Hirose edge-mount 2.92mm connectors are used. The total trace length for the entire signal path is roughly 6.2 inches (fixture + DUT). Other details can be found in Table 1.

Coaxial connector	Hirose edge-mounted 2.92mm connector
Fixture trace width, spacing to GND	5.75mils, 8mils
Fixture trace length	1.4”
DUT S/E trace width/spacing to GND	5mils, 8mils
DUT diff trace width/spacing to GND	4mils, 8mils
DUT diff trace spacing	6mils
DUT trace length	3.4”
PCB material	FR408
PCB rotation degree	15 degrees
PCB thickness	57mils
PCB layers	4

Table 1. Validation board PCB

Impedance marker

The proposed skew calculation method needs impedance markers to identify the edges of DUT. At the edge of each edge-mount 2.92mm connector, the contact pad gives low impedance and we make use of that impedance drop as a marker for the DUT board. For the fixture board, the contact pad's low impedance is compensated by a ground cut-out underneath (Figure 12). We ran HFSS [6] simulations to optimize the cut-out area for smooth impedance transition for the fixture board.

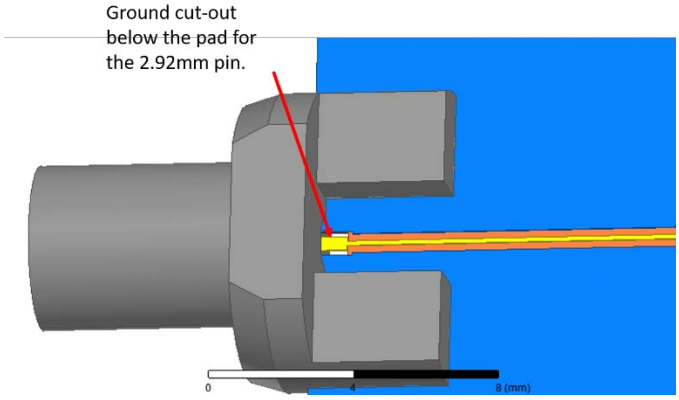

Figure 12. Optimized cut-out for Hirose 2.92mm edge-mount connector.

Test result of validation vehicle

Figure 13 (left) shows the Fixture + DUT impedance profile with 5ps rise time (20/80) and brickwall filter. All subsequent TDR and TDT graphs will follow the same setup. With optimized 2.92mm edge-mount connector pad on the fixture board, there is no large impedance drop near its edges. On the other hand, without an optimized cut-out, there are two distinct impedance drops at the DUT board which will be used as markers.

First, we measured the DUT only board and computed Skew@DUT by directly subtracting the delay between two impedance markers (Figure 13 (right)). This gives reference Skew@DUT = 0.0845ps.

Following the aforementioned procedures, we get T1=0.44147ps (Figure 14), T2=0.604554ps (Figure 15) and T3=-0.2471ps (Figure 16). Then, the proposed IFSS method gives

$$\text{Skew@DUT} = T2 + T3 - T1 = 0.604454 - (-0.2471) + 0.44147 = -0.08389ps$$

Compared with the reference, the difference is only 0.16839ps.

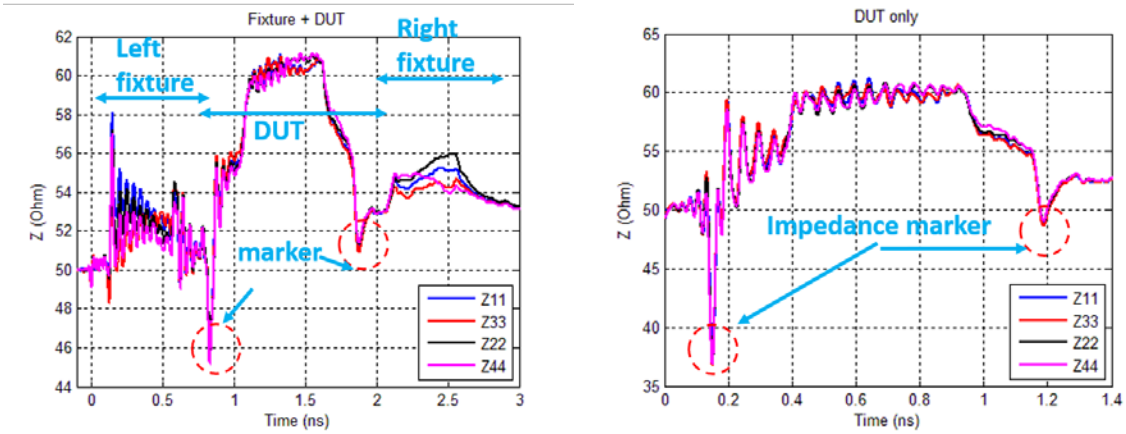

Figure 13. TDR of fixture + DUT and DUT board only.

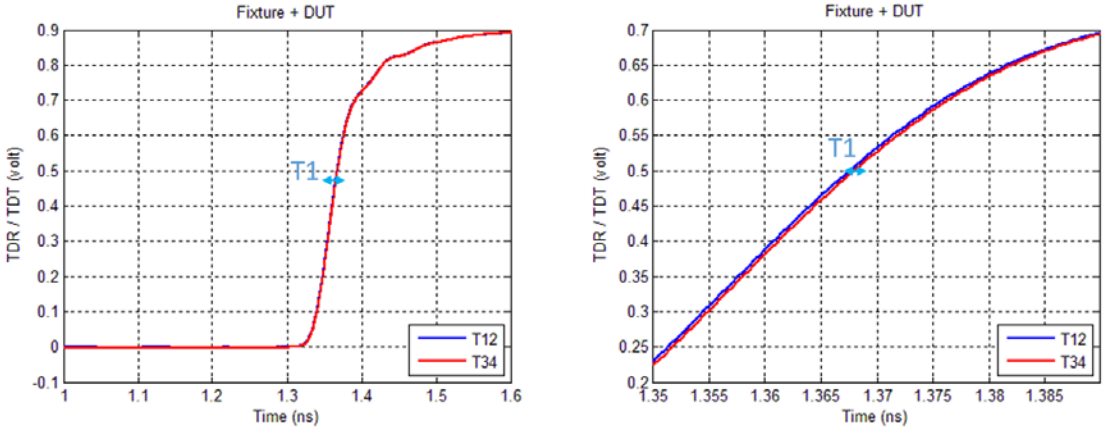

Figure 14. Computing total skew (T1) of fixture + DUT from TDT.

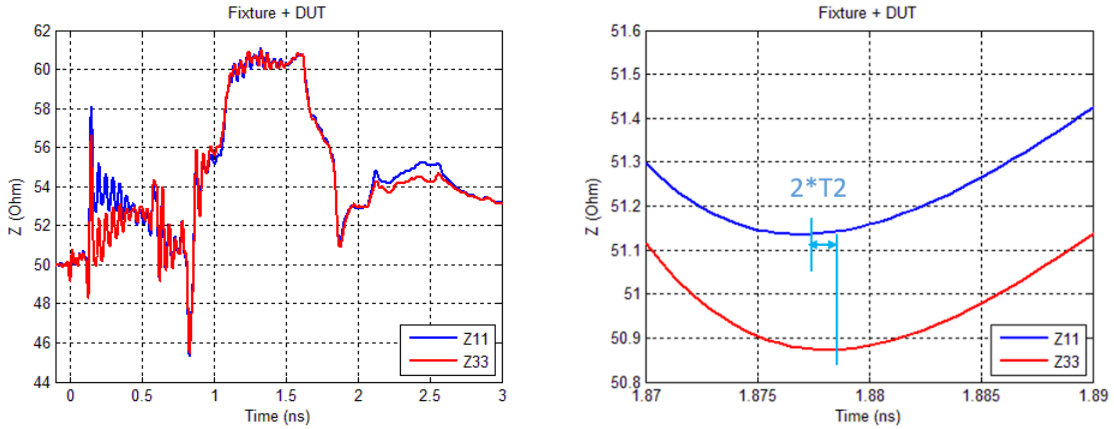

Figure 15. Computing total skew (T2) of left fixture + DUT from TDR.

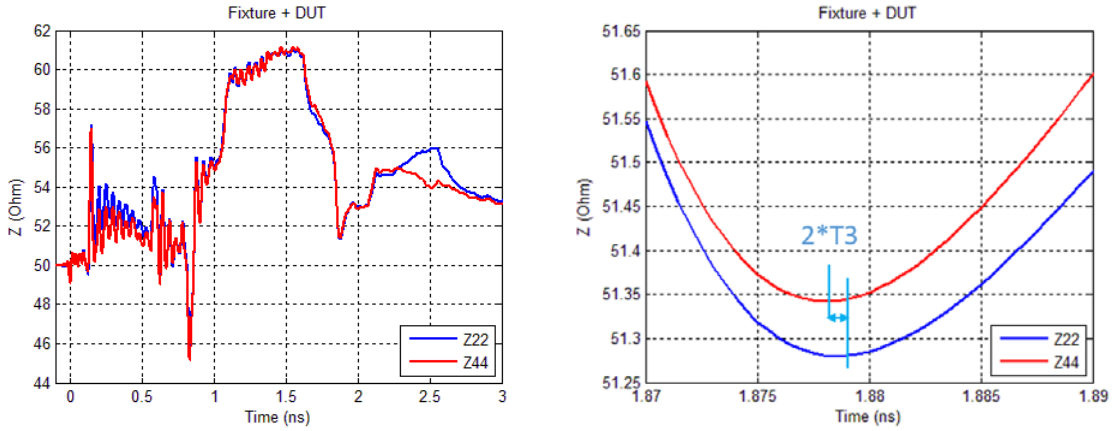

Figure 16. Computing total skew (T3) of right fixture + DUT from TDR.

Simulation

Connector example

To see if the proposed IFSS method is applicable to more complex devices other than PCB traces, we consider the simulation results of Hirose IT8, a high-speed BGA connector (Figure 17). In this example, DUT is the simulated IT8 model and the fixtures are 1.5 inches traces. The fixture + DUT model is created by cascading traces with IT8 model.

To provide maximum mechanical flexibility, IT8 is designed as a 3-piece connector with two receptacles. The slightly higher impedance in each receptacle is used as an impedance marker.

As a reference, we measured the IT8 only TDT and computed Skew@DUT at 50% of settling voltage. Using 5ps rise time (20/80) and brickwall filter, we found Skew@DUT = -0.09635ps. Figure 18 shows the phase delay of T12 and T34.

Following the aforementioned procedures, we get T1=–0.11992ps (Figure 19), T2=–0.24133ps (Figure 20) and T3=–0.11589ps (Figure 20). Then,

$$\text{Skew@DUT} = T2 + T3 - T1 = -0.24133 - 0.11589 - (-0.11992) = -0.2373ps$$

Compared with the reference Skew@DUT, the difference is 0.14095ps.

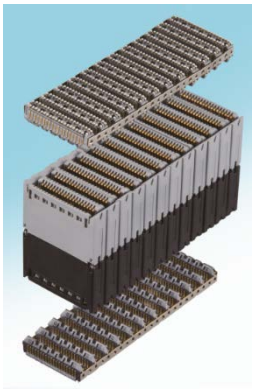

Figure 17. IT8 mezzanine connector for 56Gbps PAM4.

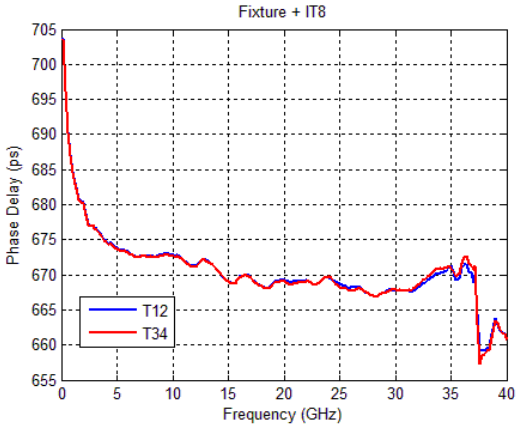

Figure 18. Phase delay of Fixture + IT8.

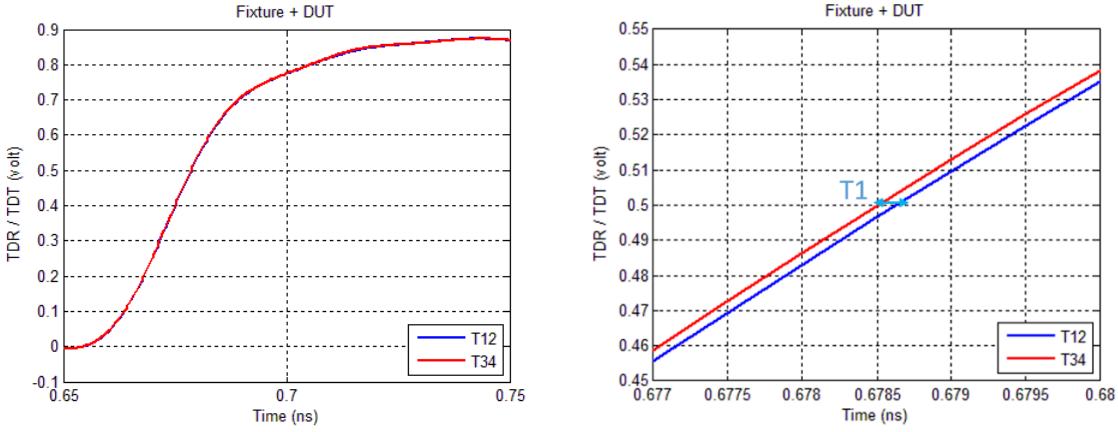

Figure 19. Computing total skew (T1) of fixture + DUT from TDT.

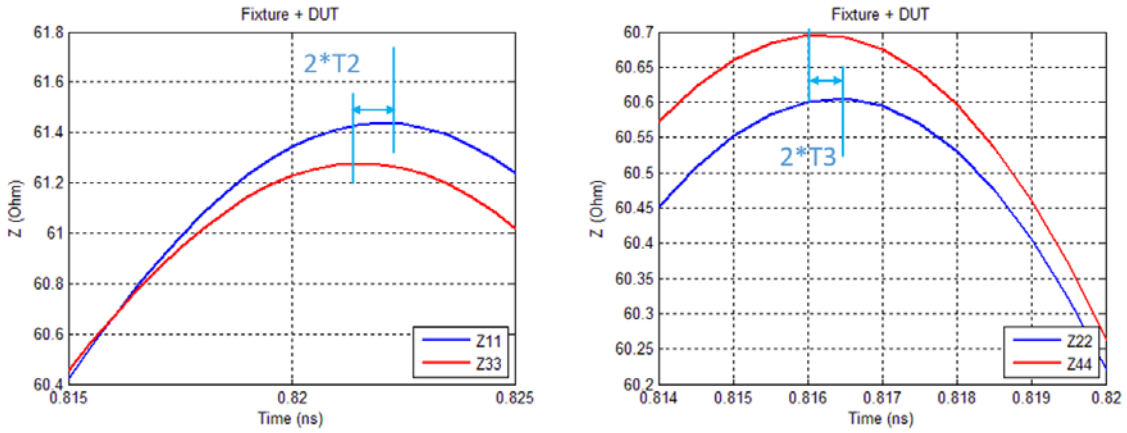

Figure 20. Computing total skew (T2) of left fixture + DUT and skew (T3) of right fixture + DUT from TDR.

Conclusion

This paper has shown how skew in fixture and/or reference coupon can affect de-embedding results. The key takeaways are:

1. Because skews in fixture and reference coupon are unknown, the DUT skew can hardly be quantified through de-embedding. When fixture and reference coupon have opposite skew, de-embedding reference coupon directly from fixture will result in even more error in DUT skew.

2. The prevalent method of de-embedding shorter traces from longer traces to get per-inch differential insertion loss must be executed with de-skewing in order to get accurate and unbiased results.

3. A new methodology, dubbed In-Fixture Skew Subtraction (IFSS), was proposed to quantify DUT skew without de-embedding. A simple equation has been derived to compute both PCB and DUT skews for those cases where DUT has distinguishable impedance discontinuities.

4. A test vehicle, consisting of three separately measurable boards with PCB traces, was made to validate the proposed IFSS method. An uncertainty of DUT skew at only ~0.168ps was observed.

5. To see if the proposed IFSS method is applicable to more complex devices other than PCB traces, we studied the simulation results of Hirose IT8, a high-speed BGA connector. Relatively small uncertainty of DUT skew at ~0.14ps was found.

6. The eventual goal is to include skew information from the proposed IFSS method, for example, in de-embedding to give more accurate DUT results.

Reference

[1] A. Nagao, T. Takada, C.C. Huang, J. Buan, K. Aihara, P. Li and A. Mihara, “New methodologies for 25+ Gbps connector characterization,” DesignCon 2014, 01/28-01/31/2014, Santa Clara, CA.

[2] H. Barnes, E. Bogain, J. Moreira, J. Ellison, J. Nadolny, C.C. Huang, M. Tsiklauri, S-J Moon and V. Herrmann, "A NIST traceable PCB kit for evaluating the accuracy of de-Embedding algorithms and corresponding metric," DesignCon 2018, 01/30-02/01/2018, Santa Clara, CA.

[3] Ching-Chao Huang, “In-Situ De-embedding,” EDI CON, Beijing, China, 04/19 to 04/21/2016.

[4] In-Situ De-embedding (ISD), www.ataitec.com

[5] J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, “Aristotle: A fully automated SI platform for PCB material characterization,” DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.

[6] HFSS, www.ansys.com