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Tradeoffs between tightly and loosely coupled differential vias for multi-Gbps design

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Abstract

Optimizing vias placement to improve insertion loss, crosstalk and/or physical routing area is crucial for multi-Gbps channel design. Should tightly or loosely coupled vias be chosen in a design? This paper discusses the tradeoffs between tightly and loosely coupled vias and compares their performance through both simulation and measurement. It is shown that, while both tightly and loosely coupled vias may appear to give similar differential insertion losses, the tightly coupled vias require the intra-pair FEXT to be just right to compensate for the nulls in single-ended insertion loss. When tightly coupled vias are used and there is skew in the channel before the vias, a system designer must take care in compensating for the skew before, not after, the vias. This design rule is to ensure that single-ended insertion loss and FEXT will add in-phase to give better differential insertion loss. Simulation shows that, when 6ps skew is compensated on the opposite side of via transition, the tightly-coupled vias can incur additional 7% eye width degradation compared to the improved (i.e., less coupled) vias.

Authors Biography

Clement Luk is a Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. He is involved in high speed connector design, device and channel simulation and measurement. He received his BSCS and MSEE from University of Wisconsin-Madison.

Jeremy Buan is a Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. As an SI Engineer, he supports the development of high-speed connectors by both simulation and measurement. He gives SI/design assistance to customers by providing connector models, evaluation boards, channel simulation data and via breakout optimization. Jeremy received his BSEE and MSEE from San Jose State University.

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Ching-Chao Huang, President of AtaiTec Corp., has more than 25 years of high-speed connector, package and system design, and SI software development experience. He held such positions as advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member and he has many patents and publications. Dr. Huang received his BSEE from National Taiwan University, and MSEE and PhD from Ohio State University.

Introduction

Optimizing vias placement to improve insertion loss, crosstalk and/or physical routing area is crucial for multi-Gbps channel design. Engineers often spend days running 3D full-wave simulations to look for the proper combination of via and anti-pad diameters, the signal and ground via locations, and so on for a specific stackup, footprint and/or routing. The conventional wisdom may prefer tightly coupled vias for differential signaling. But, are tightly coupled vias really better than loosely coupled vias? This paper attempts to study the electrical characteristics of tightly and loosely coupled vias in detail.

While both tightly and loosely coupled vias may give similar differential insertion losses, notable difference can be found in single-ended insertion loss and FEXT. We explain this behavior in the Theory section by drawing a parallel to microstrip traces. In tightly coupled traces, simulated by 2D solver [1], the nulls of single-ended insertion loss are seen to coincide with the peaks of FEXT. The *FEXT induced resonance* can result in maximum FEXT leakage and minimum (single-ended) signal transmission. Fortunately FEXT from another line of the same differential pair adds constructively to the transmitted signal to give "good" differential insertion loss.

Several examples, including field-solver simulation, measurement and channel simulation, are presented in the Examples section. In Example 1, the GSSG and GSGSG pin configurations (where G=ground and S=signal) are used for tightly and loosely coupled vias, respectively. Analogous to the microstrip traces, tightly coupled vias, simulated by 3D solver [2], also exhibit nulls and peaks in single-ended insertion loss and FEXT, respectively.

In Example 2, an existing tightly coupled via design for Hirose IT8 mezzanine connector is compared to an improved design. In the improved design, an additional ground via is inserted between two signal vias to make them less coupled to each other. Simulation results show that both designs give similar differential insertion loss. However, the improved design is less sensitive to the channel's skew, especially when the skew is not compensated correctly.

In Example 3, a test vehicle with two pairs of tightly coupled microstrip traces was built and measured. These traces all have the same total length, although every trace has different length in the breakout (i.e., uncoupled) and tightly coupled sections. The VNA measurement shows that more length difference in the uncoupled (or coupled) sections results in more degradation in differential insertion loss.

In Example 4, eye diagrams for the entire channel of Example 2 are simulated [3]. Skews are added before and then compensated after the via-connector-via transition, keeping the total delay the same for every signal line. In the presence of tightly coupled vias, the jitter is found to increase more rapidly with increased skew before the transition. Simulation shows that, when 6ps skew is compensated on the opposite side of via transition, the tightly-coupled vias can incur additional 7% eye width degradation compared to the improved (i.e., less coupled) vias.

Finally, this paper arrives at a design rule that channel skew before any tightly coupled component (such as vias) must be compensated before, not after, that component. This design rule is to ensure that the single-ended insertion loss and FEXT will add in-phase to give better differential insertion loss.

Theory

FEXT induced Resonance

To help understand the difference between tightly and loosely coupled vias, let us study a pair of microstrip traces first. Using a 2D solver [1], we create S parameters for tightly and loosely coupled microstrip traces of 25mm length (Figure 1 and Figure 2).

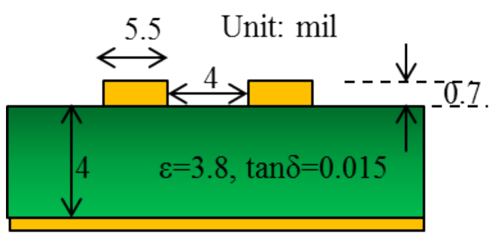

Figure 1. Tightly-coupled microstrip traces.

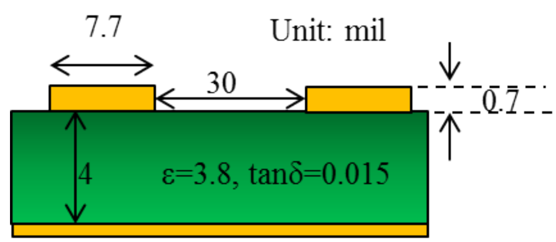

Figure 2. Loosely-coupled microstrip traces.

Apparent difference can be seen in the single-ended insertion loss (Figure 3) where nulls exist at ~35 GHz and ~105 GHz for tightly coupled traces and are absent for loosely coupled traces. Despite the difference, both tightly and loosely coupled traces give similar, linear-looking differential insertion losses (Figure 4). In the tightly coupled case, the nulls of single-ended insertion loss coincide with the peaks of intra-pair FEXT (Figure 5). Such *FEXT induced resonance* results in maximum FEXT leakage and minimum signal transmission at those frequencies.

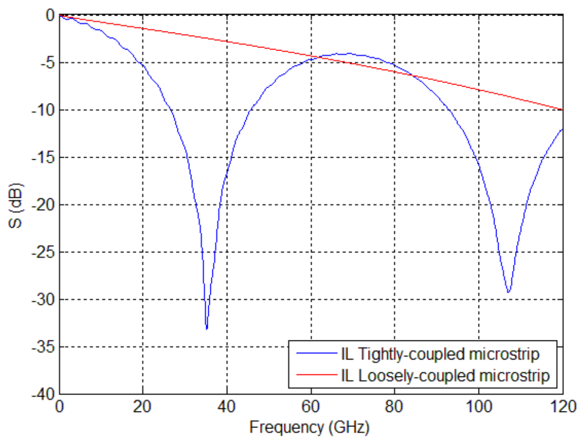

Figure 3. Single-ended insertion loss of tightly vs. loosely coupled microstrips.

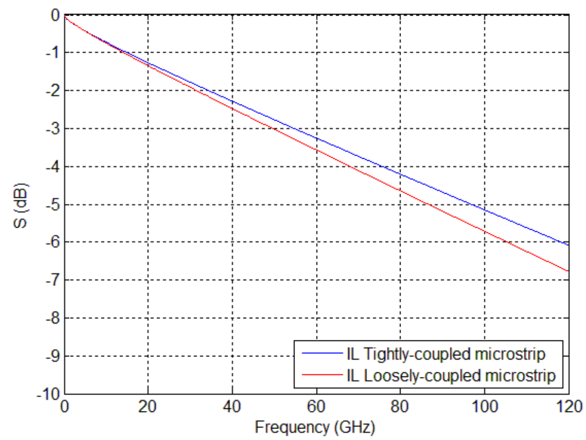

Figure 4. Differential insertion loss of tightly vs. loosely coupled microstrips.

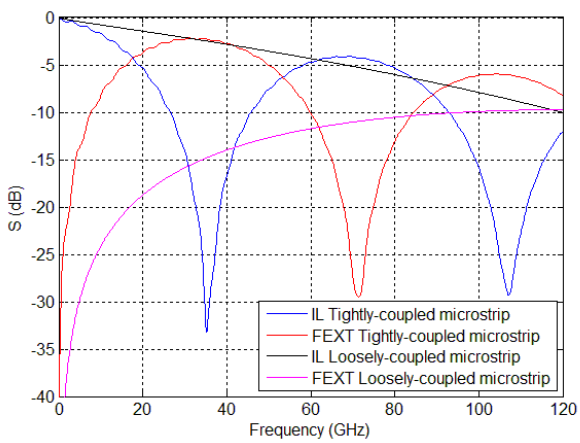

Figure 5. Intra-pair FEXT and insertion loss of tightly and loosely coupled microstrips.

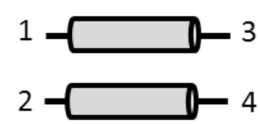

Figure 6. Port numbers of two microstrip traces.

To help understand why both tightly and loosely coupled traces give linear differential insertion losses, let us examine the equation:

$$SDD_{12} = \frac{1}{2}(S_{13} + S_{24} - S_{14} - S_{23}) \quad (1)$$

where SDD_{12} is the differential insertion loss and Ports 1 to 4 are as shown in Figure 6. In a symmetric case, SDD_{12} is simply the difference between single-ended insertion loss and FEXT:

$$SDD_{12} = S_{13} - S_{14} \quad (2)$$

In this tightly-coupled microstrip example, the single-ended insertion loss and intra-pair FEXT are ~164 degrees out of phase when the insertion loss is at its first null (Figure 7 and Figure 8). Effectively, the intra-pair FEXT is added back to make the differential insertion loss a smooth curve (Figure 4).

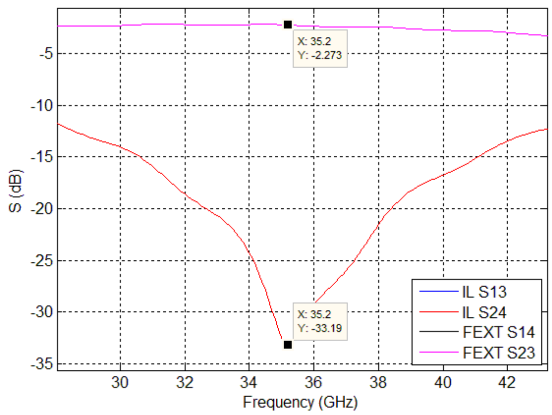

Figure 7. Tightly-coupled microstrip magnitude.

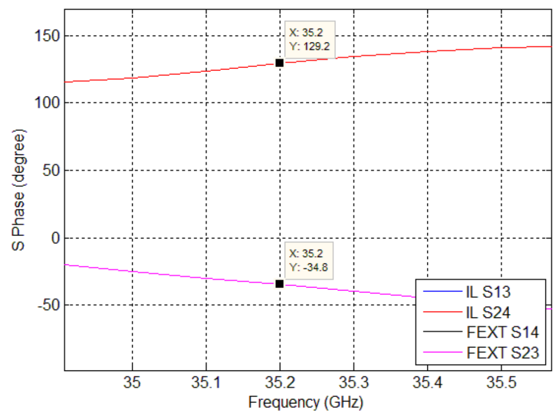

Figure 8. Tightly-coupled microstrip phase.

Examples

Example 1. Tightly vs. loosely-coupled vias

Observation from the previous section can be used to explain the behavior of tightly and loosely coupled vias as well. In this example, we compare tightly and loosely coupled vias in GSSG and GSGSG pin configurations, respectively. In the tightly coupled case (Figure 9), 11.5mil signal via drill, 40mil anti-pad and 14mil ground via drill are used. In the loosely coupled case (Figure 10), 10mil signal via drill, 39mil anti-pad and 14mil ground via drill are used. The board is 129mil thick with 28 layers and the via is 112mil long (exiting at layer 25) with 8.4mil stub. The single-ended insertion loss, FEXT and differential insertion loss are shown in Figure 11 to Figure 12, which bear strong resemblance to Figure 3 to Figure 5. For single-ended S-parameter, Ports 1 and 2 are on the BGA side and Ports 3 and 4 at the exit of inner layer traces. For differential S-parameter, Pair 1 is on the BGA side and Pair 2 is at the exit of inner layer traces.

That both tightly and loosely coupled vias give similarly smooth differential insertion loss even though their single-ended insertion losses exhibit very different behavior can be explained by their time domain responses as well. Assuming a step input of 1 volt swing and 20ps rise time (20% to 80%), TDT gives -5.7mV and -95mV intra-pair FEXT (Figure 13 to Figure 15) for tightly and loosely coupled vias, respectively. The much larger intra-pair FEXT in time domain for tightly coupled vias corresponds directly to the much larger intra-pair FEXT in frequency domain. Because FEXT is usually of opposite polarity to the input signal, the positive signal couples negatively to the negative signal and the negative signal couples positively to the positive signal (Figure 16), effectively "patching up" the transmitted single-ended signals and reducing the distortion of transmitted differential signal.

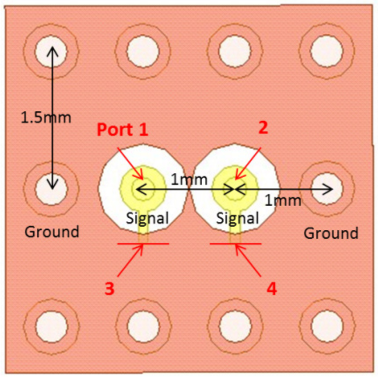

Figure 9. Tightly-coupled vias.

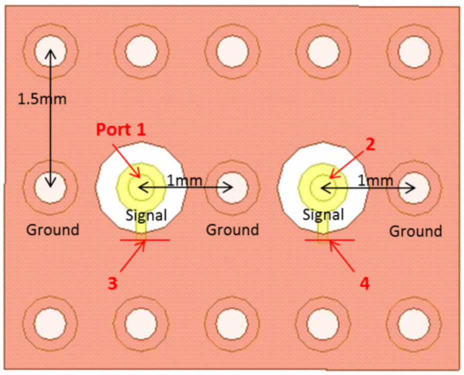

Figure 10. Loosely-coupled vias.

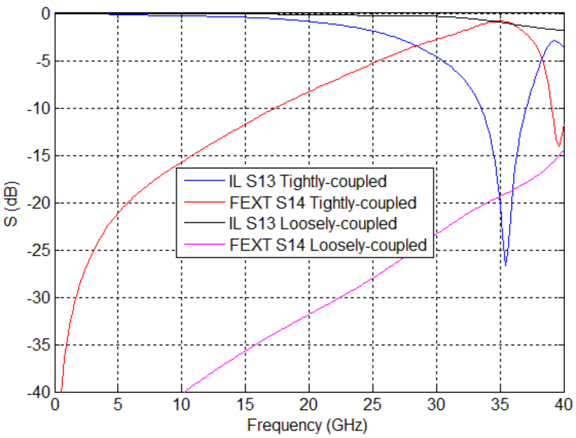

Figure 11. Single-ended IL, FEXT of tightly vs. loosely-coupled vias.

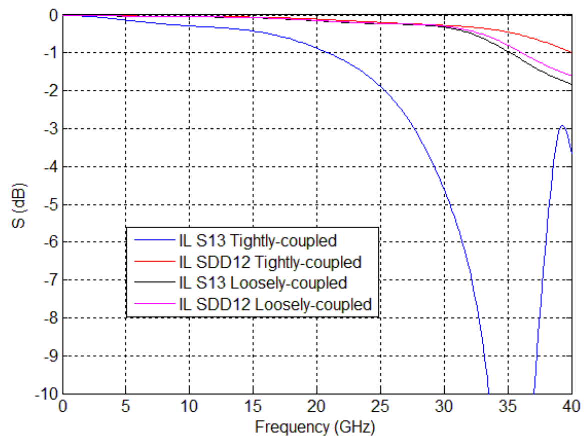

Figure 12. Single-ended vs. diff IL of tightly vs. loosely-coupled vias.

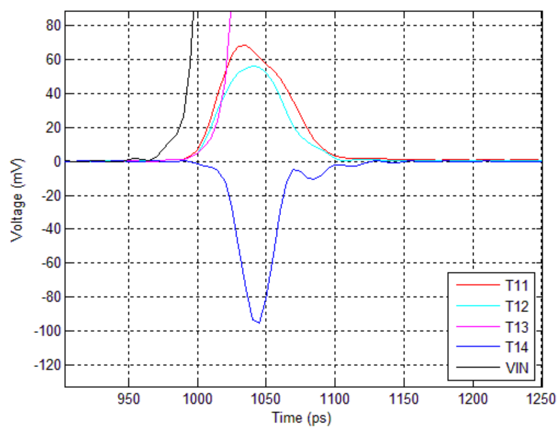

Figure 13. TDR/TDT of tightly-coupled vias at port 1.

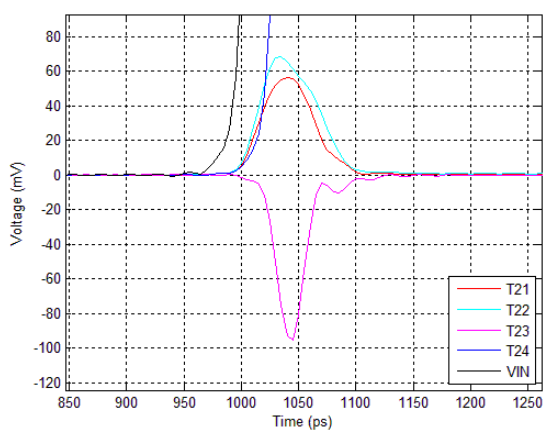

Figure 14. TDR/TDT of tightly-coupled vias at port 2.

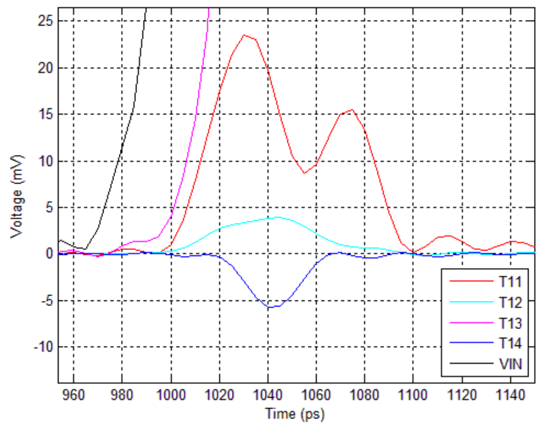

Figure 15. TDR/TDT of Loosely-coupled vias at port 1.

Figure 16. Illustration of how differential signal is "recovered".

Example 2. Optimizing via design for a 56Gbps mezzanine connector

In this example, two via designs for Hirose's IT8 mezzanine connector (Figure 17) are studied. Tightly coupled vias (Figure 18), with 1mm pitch both between signals and between signal and ground, are used in the first design. In the second "improved" design (Figure 19), a small ground via (of 9mil drill) is inserted between the signal vias to make them less tightly coupled.

The board is 129mil thick with 28 layers and the via is 112mil long (exiting at layer 25) with 8.4mil stub. Similar to the loosely-coupled vias in Example 1, the single-ended insertion loss of "improved" design is free of sharp drops within the frequency range of interest (Figure 20). For single-ended S-parameter, Ports 1 and 2 are on the BGA side and Ports 3 and 4 are at the exit of inner layer traces. For differential S-parameter, Pair 1 is on the BGA side and Pair 2 is at the exit of inner layer traces.

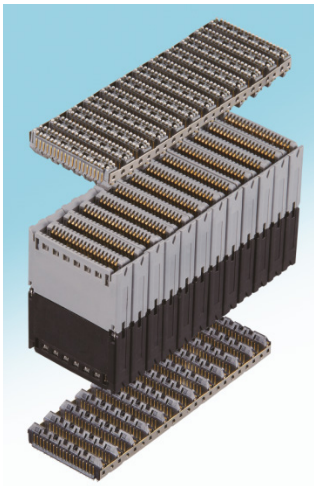

Figure 17. Hirose IT8 mezzanine connector.

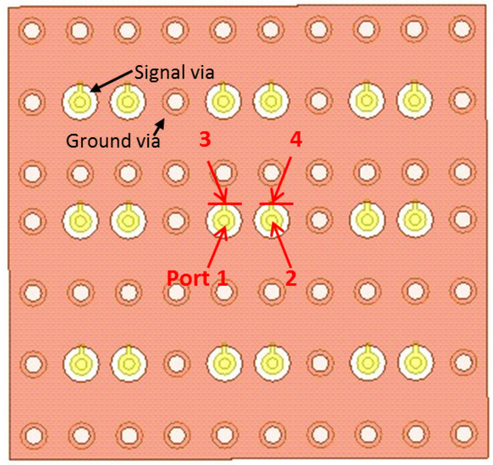

Figure 18. Tightly-coupled via design.

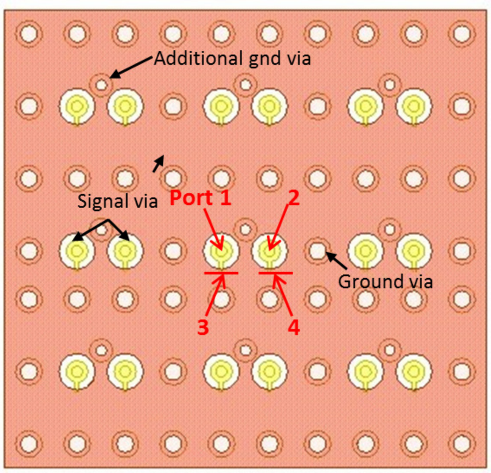

Figure 19. Improved via design.

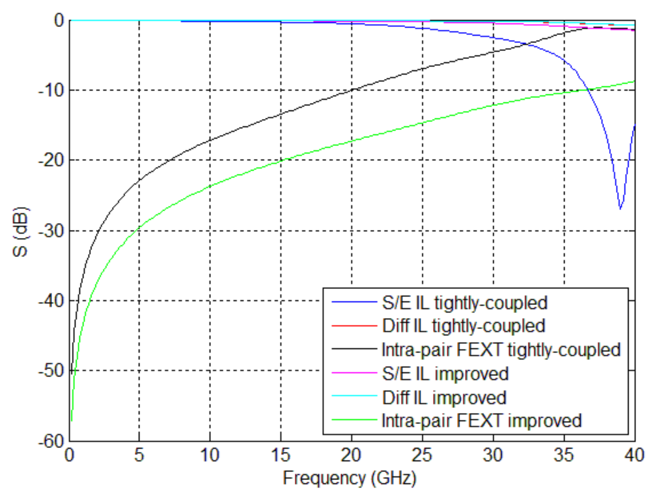

Figure 20. IL and FEXT of tightly-coupled and improved vias.

<u>Effect of skew</u>

While both tightly coupled and improved vias give similar differential insertion loss in Figure 20, the former can actually be more sensitive to the channel skew. Figure 21shows one configuration where skew before the vias is compensated by adding delay after the vias. Though two signal lines are now delay matched, the tightly coupled vias give worse differential insertion loss for the same original skew (Figure 22).

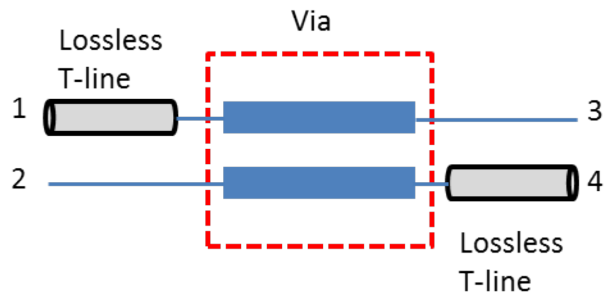

Figure 21. Setup to study the effect of skew.

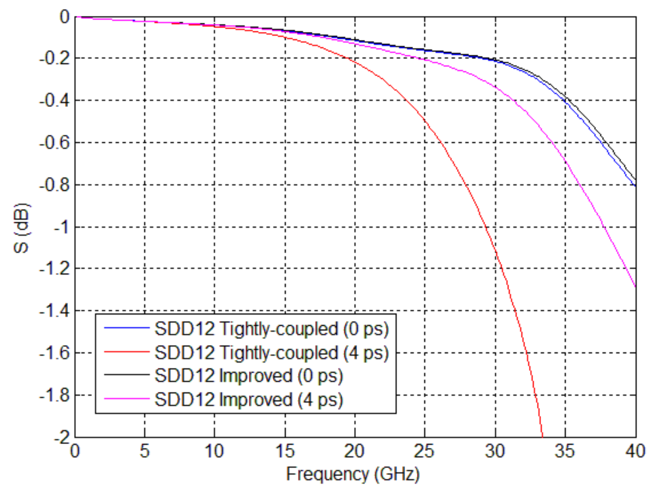

Figure 22. Differential insertion loss with/without skew for tightly coupled vs. improved vias

Why are tightly-coupled vias subject to more insertion loss degradation with skew? Let us explain this by Eq. (1) again. For tightly-coupled vias, the drop in single-ended insertion loss is compensated by increase in FEXT. However, with delays added to Ports 1 and 4, the intra-pair FEXTs (S_{14} and S_{23}) are no longer symmetric because Port 1 to 4 is a longer path than Port 2 to 3. As a result, there is phase shift between S_{14} and S_{23} and the single-ended insertion loss is not compensated by intra-pair FEXT.

The sensitivity of SDD12 to the skew for tightly-coupled vias is shown in Figure 23 and Table 1. Table 1 shows that, with 5ps skew, the tightly-coupled vias have additional 0.49 dB loss at 25 GHz.

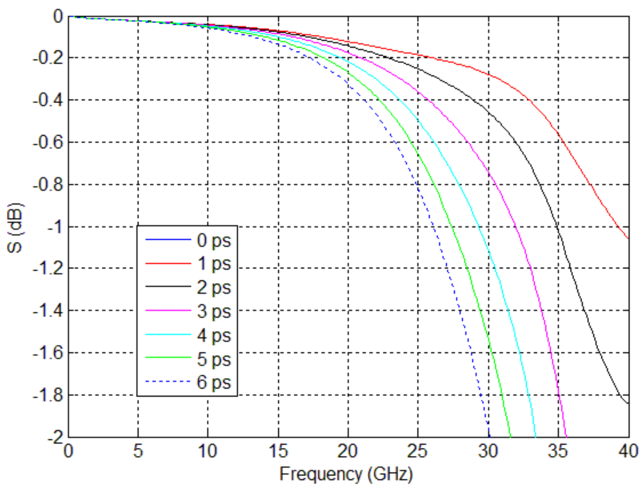

Figure 23. Sensitivity of SDD12 to skew for tightly-coupled vias.

Skew (ps)	IL (dB)
1	0.19
2	0.25
3	0.36
4	0.50
5	0.66
6	0.82

Table 1. Differential IL of tightly coupled vias vs. skew at 25GHz.

Mode conversion

Using the same setup in Figure 21, we also investigate the common-to-differential conversion for insertion loss. The tightly-coupled vias show more mode conversion with skew than the improved vias (Figure 24). Let us examine the definition of mode conversion (SDC_{12}) to understand why this is the case:

$$SDC_{12} = \frac{1}{2}(S_{13} + S_{14} - S_{23} - S_{24}) \tag{3}$$

For tightly-coupled vias, S_{13} and S_{24} are somewhat symmetric so they cancel out each other. However, due to different delays, S_{14} and S_{23} do not cancel and their difference shows up as mode conversion. For the improved vias, different delays also affect S_{14} and S_{23}, but because their values are smaller, the mode conversion is less.

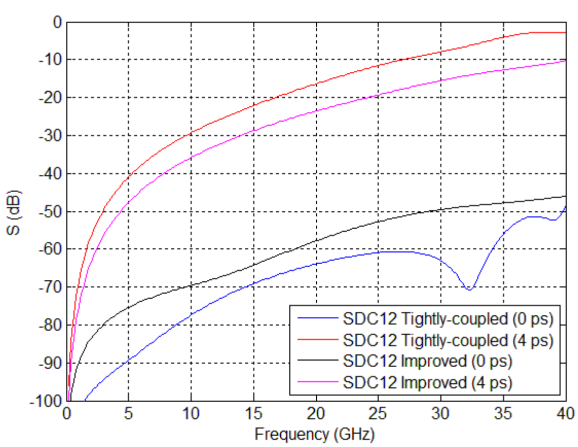

Figure 24. Skew effect on mode conversion for tightly vs. improved vias

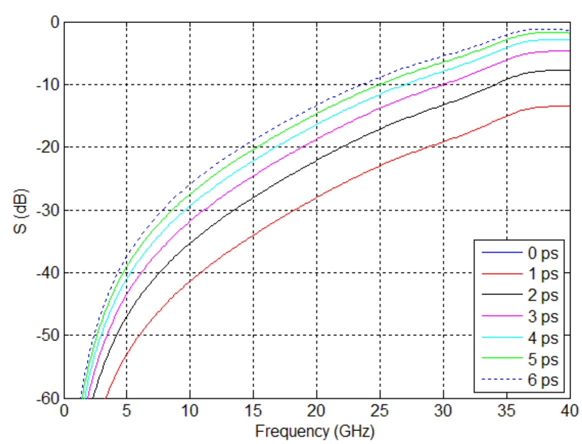

Figure 25. Sensitivity of mode conversion to skew for tightly-coupled vias

Example 3. Measurement validation

In this example, we use a test vehicle (Figure 26 to Figure 27) to show how difficult it is to compensate for the skew in tightly-coupled microstrip traces.

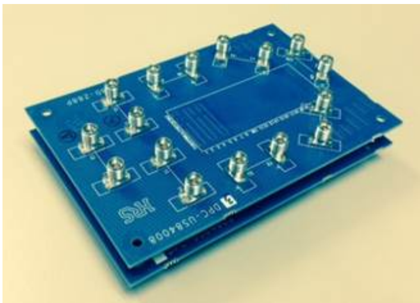

Figure 26. Test vehicle.

Coax connector	2.92mm connector
Coax conn via stubs	None
Trace design	Tightly coupled microstrip
Trace length	5.64” (2.82”+2.82”)
Dielectric material	FR408HR
Gerber rotation	15 degrees
PCB thickness	60mils
# Copper layers	6
Vias stub	None

Figure 27. Construction of test vehicle.

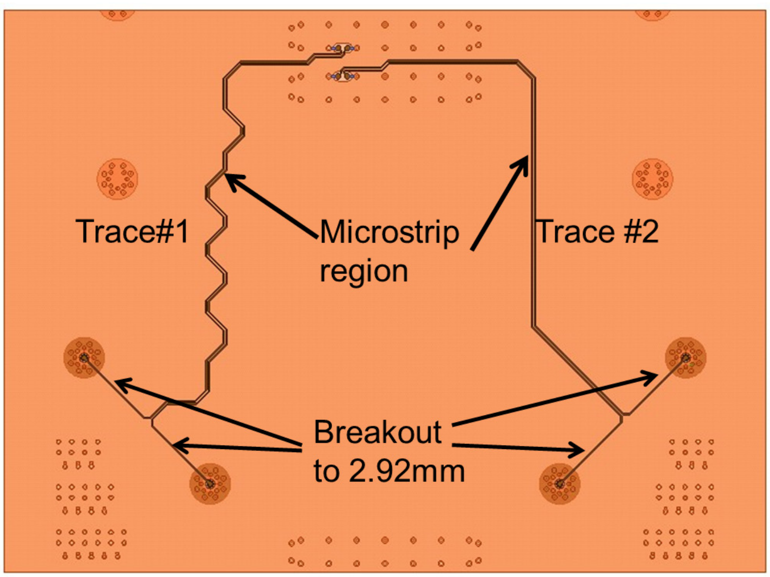

Figure 28. Board layout.

Figure 29. Layout showing the breakout to 2.92mm connectors.

In Figure 28 to Figure 29, both traces 1 and 2 are routed as tightly-coupled microstrips until the breakout region, and the total lengths are matched to be 2.82”. At the breakout region to 2.92mm connectors, the traces to the left and right use slightly different lengths to match the differences due to the bending of the tightly coupled sections. Whenever a differential pair bends at a 45 degree angle, the trace on the inside of the bend becomes shorter than the trace on the outside of the bend. The trace lengths are shown in Figure 30 where difference in the tightly-coupled region is compensated by the breakout section to 2.92mm connectors.

Unit in mils	Breakout section of “+” line	Breakout section of “-” line	Total length of “+” line	Total length of “-” line
Trace#1	345.62	355.74	2819.22	2819.18
Trace#2	366.01	335.92	2819.20	2819.18

Figure 30. Length of traces #1 and #2.

The measured differential insertion loss of Figure 26 (i.e., 2.92mm connector + 2.82” trace + Hirose IT8 mezzanine connector + 2.82” trace + 2.92mm connector) is shown in Figure 31. The measured result shows that trace #2 with more length difference in the breakout region results in more degradation in insertion loss due to skew and mode conversion.

The above observation has crucial implication for practical layouts in that skew in tightly coupled traces CANNOT be fully compensated by padding isolated traces. The reason is, the asymmetry makes the intra-pair FEXTs not cancel each other in Eq. (3), resulting in mode conversion and energy loss.

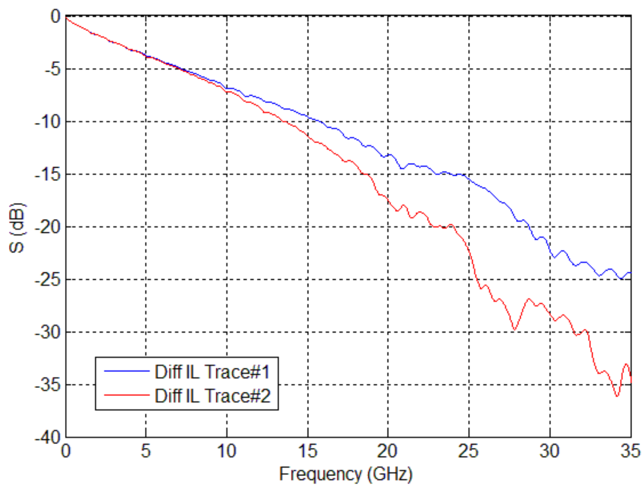

Figure 31. Measured differential insertion loss of traces #1 and #2.

Example 4. Channel simulation

To study the effect of skew on voltage and timing margins, we simulate the channel (Figure 32) that consists of vias (in the motherboard), Hirose IT8 connector, and vias (in the daughter card). Similar to Figure 21, we add delay to Port 1 and compensate the delay at Port 4. The delay at Port 4 can be compared to a de-skewing circuit at the receiver. Two different channel lengths (3"+3" and 6"+6") were simulated at 50 Gbps NRZ with 1 volt swing (peak-to-peak), PRBS12, 3-tap FFE, CTLE and 3-tap DFE. The eye diagrams are shown in Figure 33 to Figure 40 and the eye height, eye width, and jitter are summarized in Table 2 and Table 3. The additional degradation due to 6ps skew using tightly-coupled vias as compared to improved vias is shown in Table 4.

In the 3"+3" channel, it is shown that by compensating 6ps skew after the vias, the eye width incurred additional 0.496ps degradation. Using the eye width spec. of 0.35UI as reference [4], the 0.496ps additional degradation is equivalent to 7% eye width reduction. With carefully designed vias, the saving in eye width can be budgeted for other components in the channel. This shows how a good via design can have significant impact to a channel's performance.

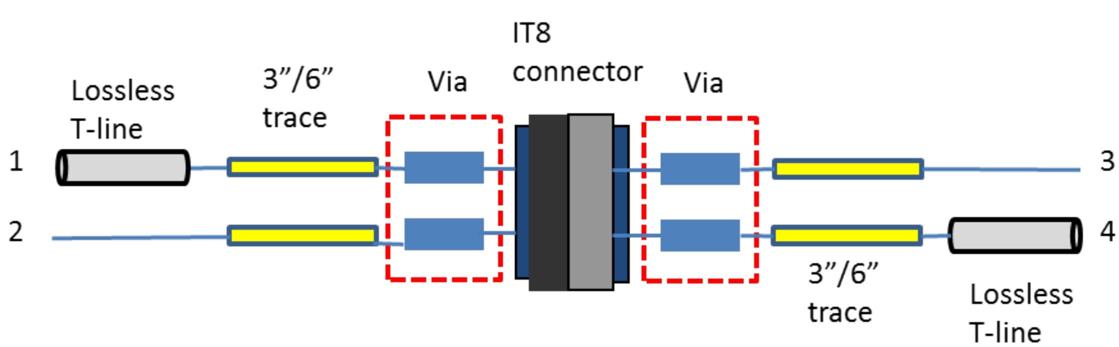

Figure 32. Channel setup for tightly-coupled vs. improved vias with added skew.

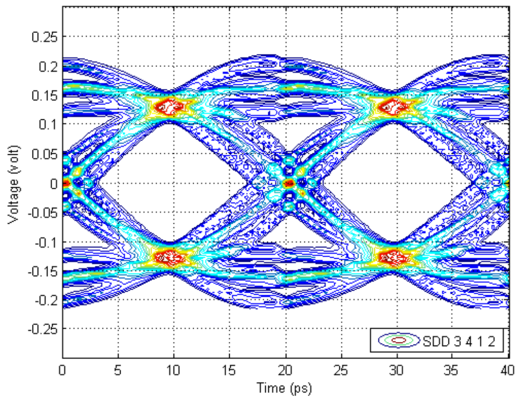

Figure 33. 0ps skew in a 3”+3” channel with tightly-coupled vias.

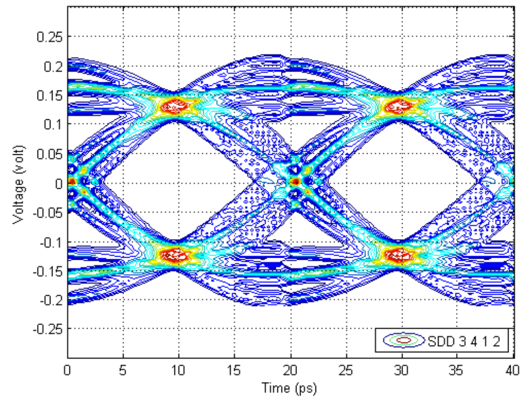

Figure 34. 0ps skew in a 3”+3” channel with improved vias.

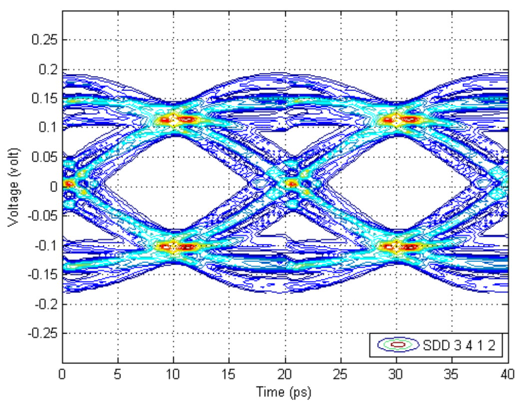

Figure 35. 6ps skew in a 3”+3” channel with tightly-coupled vias.

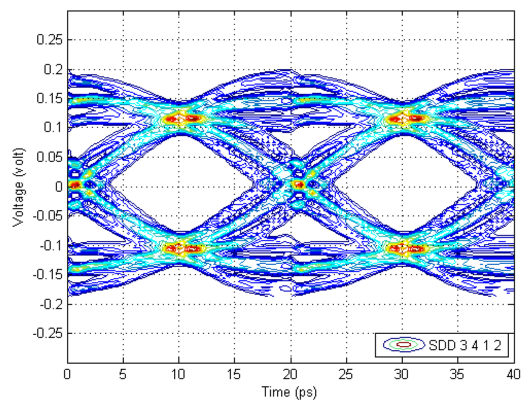

Figure 36. 6ps skew in a 3”+3” channel with improved vias.

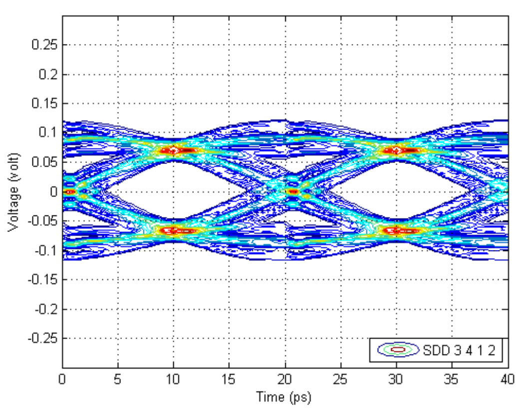

Figure 37. 0ps skew in a 6"+6" channel with tightly-coupled vias.

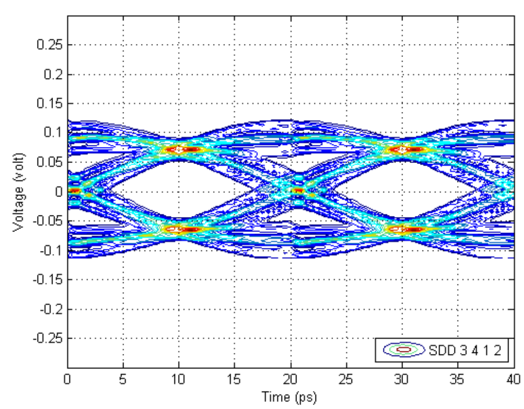

Figure 38. 6ps skew in a 6"+6" channel with improved vias.

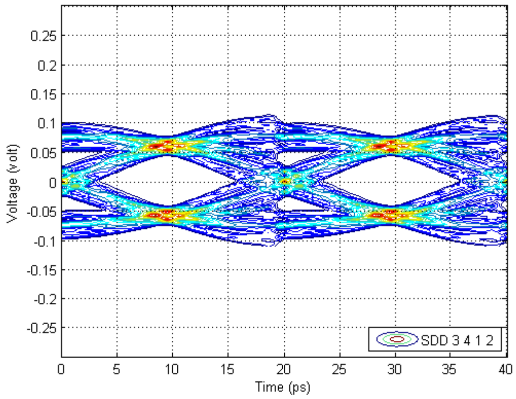

Figure 39. 6ps skew in a 6"+6" channel with tightly-coupled vias.

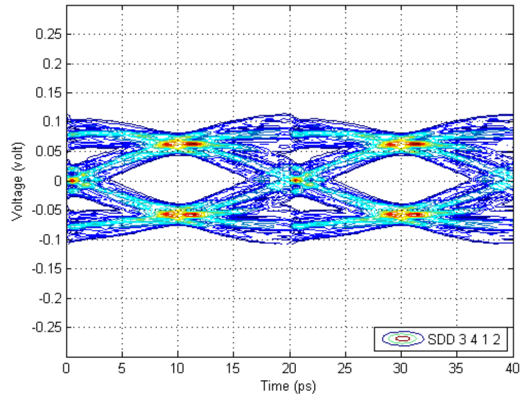

Figure 40. 6ps skew in a 6"+6" channel with improved vias.

	Tightly-coupled vias			Improved vias		
Skew (ps)	EH (mV)	EW (ps)	Jitter (ps)	EH (mV)	EW (ps)	Jitter (ps)
0	195.038	12.834	7.166	195.587	12.646	7.354
6	161.099	12.050	7.950	166.557	12.359	7.641
Delta	33.939	0.784	0.784	29.030	0.287	0.287

Table 2. 3”+3” channel simulation with tightly-coupled vs. improved vias.

	Tightly-coupled vias			Improved vias		
Skew (ps)	EH (mV)	EW (ps)	Jitter (ps)	EH (mV)	EW (ps)	Jitter (ps)
0	99.792	12.090	7.910	98.726	11.767	8.233
6	79.037	11.147	8.853	79.643	11.201	8.799
Delta	20.754	0.943	0.943	19.083	0.566	0.566

Table 3. 6"+6" channel simulation with tightly-coupled vs. improved vias.

	Additional Degradation		
Traces	EH (mV)	EW (ps)	EW relative to 0.35UI
3"+3"	4.909	0.496	7.091%
6"+6"	1.671	0.377	5.381%

Table 4. Additional degradation by using tightly-coupled vias instead of improved vias when there is 6ps skew.

Conclusion

Tightly coupled vias exhibit sharp drops in single-ended insertion loss at high frequencies (> 35 GHz). These sharp drops were found analogous to the FEXT induced resonance in tightly coupled microstrip traces. To alleviate such sharp drops, an extra ground via was inserted between two tightly coupled signal vias. This "improved" design makes the vias less tightly coupled and the entire channel less susceptible to the adverse effects of skew, albeit at the expense of routing space. The tradeoffs between tightly-coupled and improved via designs are summarized in the following table.

	Tightly-coupled vias	**Improved vias**
Single-ended signals	Large dip in insertion loss	Smooth insertion loss curve
Differential signals	Smooth insertion loss curve	Smooth insertion loss curve
Density	High density	Reduced density
Routing	Maximum routing space	Reduced routing space
Skew	More susceptible to skew	Less susceptible to skew
Mode conversion	More susceptible to SDC loss	Less susceptible to SDC loss

This paper has shown that the differential insertion loss is degraded by the skew between two single-ended signals. In addition, the skew that occurs before tightly coupled vias can only be properly compensated by adjusting delay before, not after, those tightly coupled vias, and vice versa.

The same conclusion is applicable to any tightly coupled component in a channel. When a channel consists of a tightly coupled component, it is helpful to insert a retimer before that component. Simulation shows that, when 6ps skew is compensated on the opposite side of via transition, the tightly-coupled vias can incur additional 7% eye width degradation compared with improved (i.e., less coupled) vias. This shows how a good via design can have significant impact to a channel's performance.

Reference

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