Recent Advances in Extracting DK, DF & Roughness of PCB Material

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This session was presented as part of the DesignCon 2019 Conference and Expo

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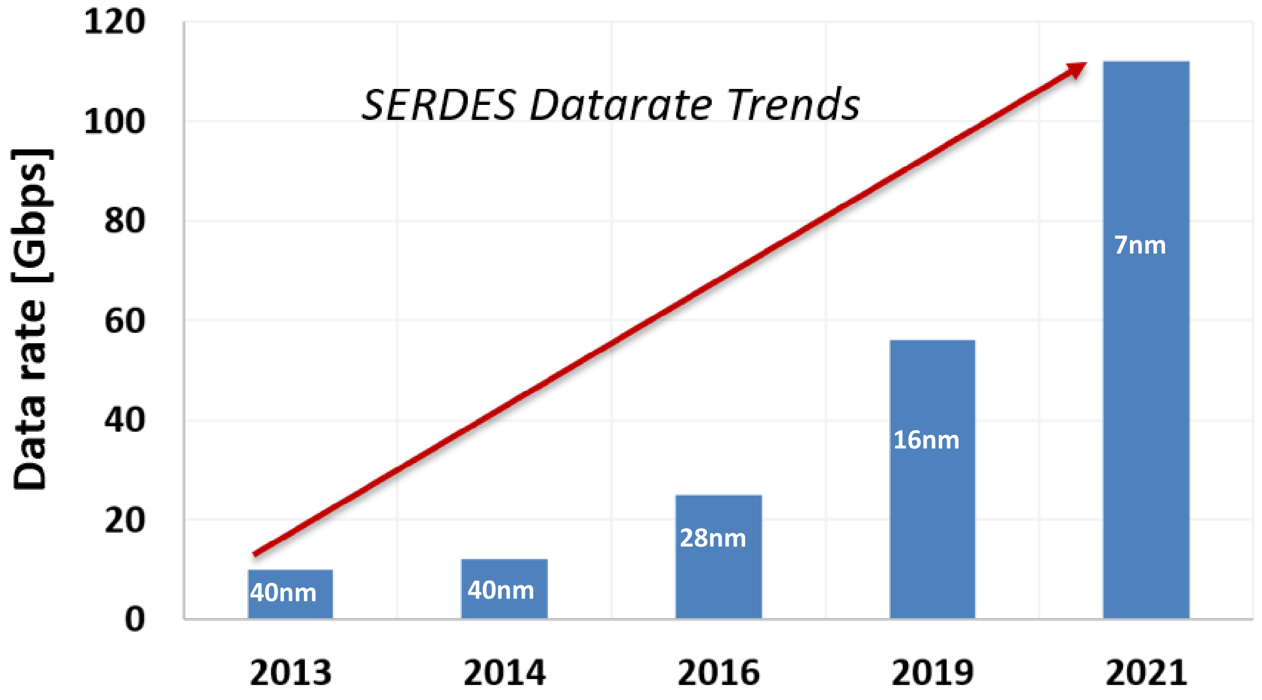
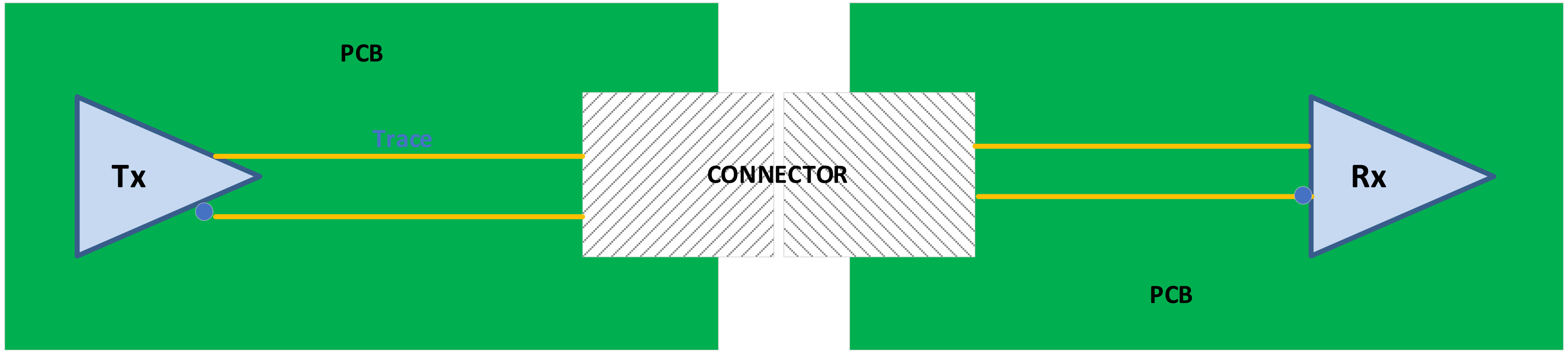
Relentless IO BW increase Pushes PCB design to Limits



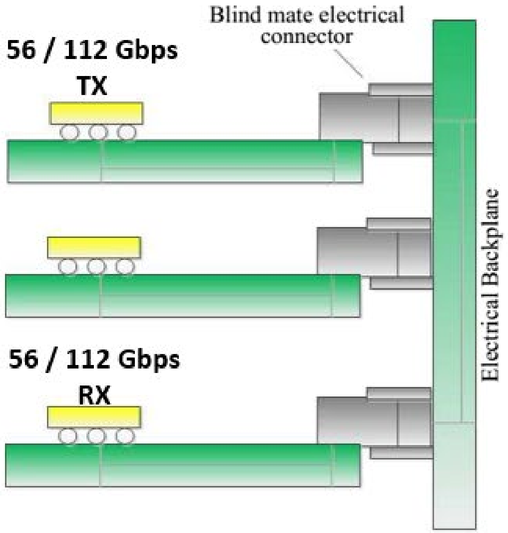
PCB Design Challenge

Top of Mind PCB design Questions

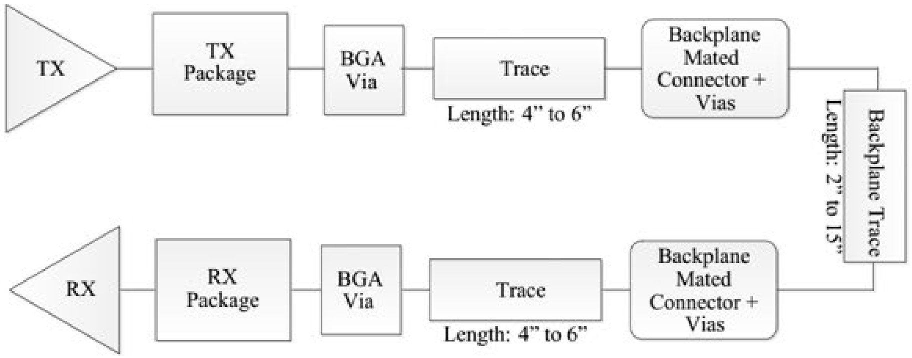


a. What dielectric to choose ?
b. What type of Cu foil to use – Rough, smooth, ultra smooth ?
c. How long can the traces be ?
d. Does it have right impedance ?
e. Does it have sufficient margin for High Volume Manufacturing ?
f. How dense can the layout be ?
g. Will my design work with fabs both X and Y ?

Electrical Backplane Example



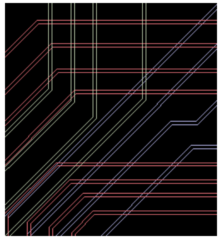
Physical Structure



Composite Channel Model

PCB Design Signal Integrity Verification Flow

Geometry



Field Solver

Stackup Parameters
Trace, dielectric thickness

Material Properties
Cu Conductivity
Dk, Df

System Simulator
SPICE, Statistical

Composite Channel Model

FD Metrics – ICR, RL, IL
TD Metrics – Eye Width, Eye height

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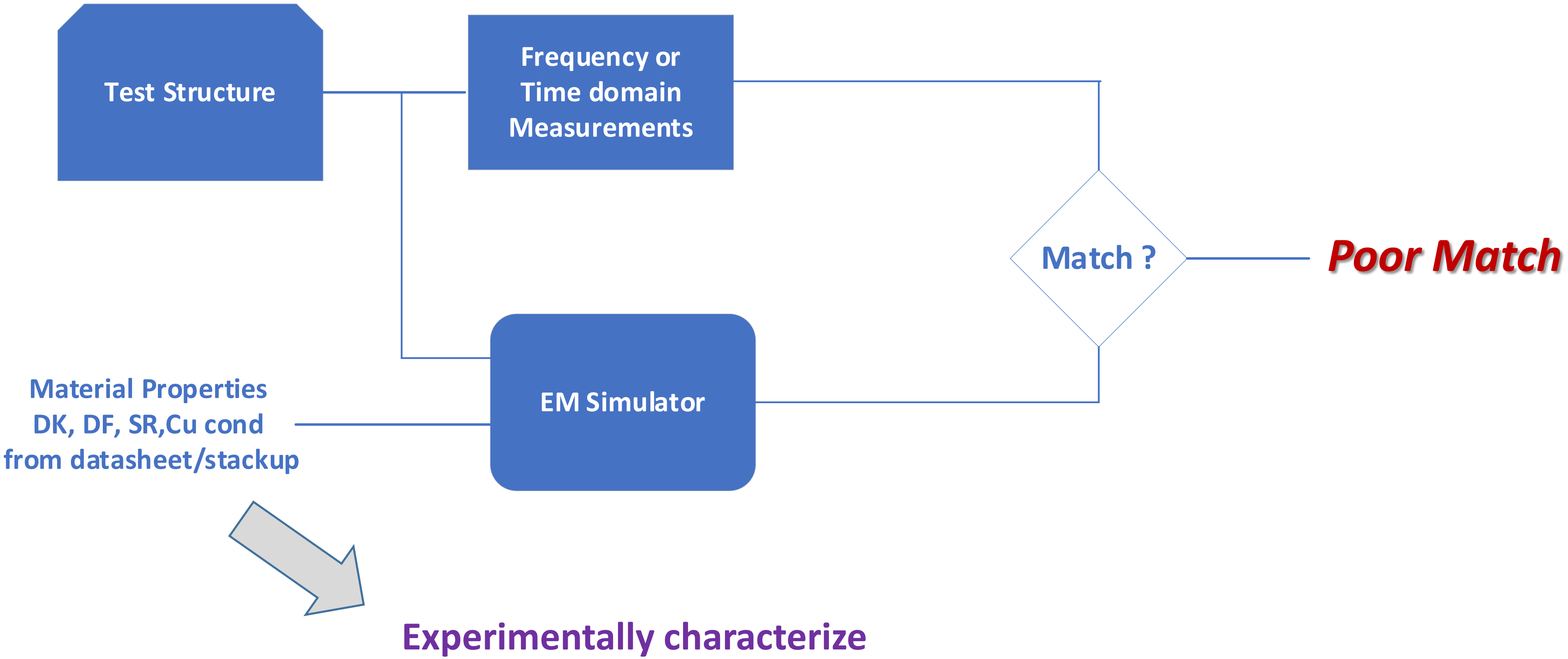
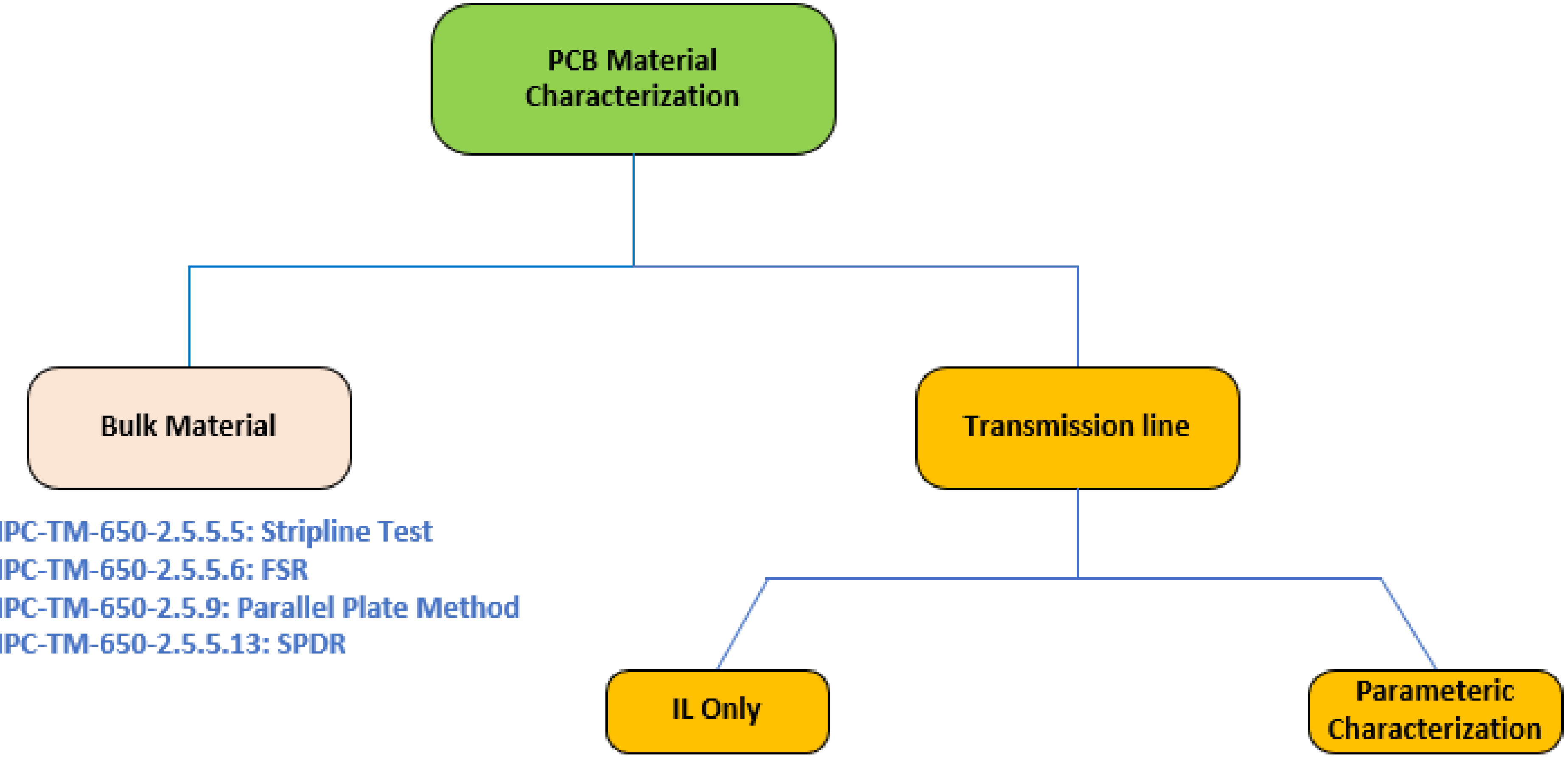
WHERE THE CHIP MEETS THE BOARD

PCB Interconnect Performance Prediction requires Meticulous Characterization of Material Properties



PCB Material Characterization Methods



Bulk Material

- IPC-TM-650-2.5.5.5: Stripline Test
- IPC-TM-650-2.5.5.6: FSR
- IPC-TM-650-2.5.9: Parallel Plate Method
- IPC-TM-650-2.5.5.13: SPDR

IL Only

- IPC D24D
- Delta - L
- SET2DIL

Parameteric Characterization — DK, DF, SR, IL

- SPP
- Tline Resonator – Beaty lines, T structures
- Gamma-T
- Fixture de-embedding → AFR, ISD

IEEE P370 Charter

This tutorial focus

DesignCon 2019 — Where the chip meets the board

Material Property Extraction Challenges

- Material properties change with the test method
- Dielectric and surface roughness models not consistent across EM simulators → hidden parameters with unknown values
- Ambiguity in separation of dielectric and conductor losses
- Fixture design for very high bandwidth
- Material property extraction – a big data problem

PCB Material Characterization Requirements

- Material properties over wide bandwidth
- Causal, Passive response
- Well correlated with measurements
- Consistent and repeatable test method
- Characterization on the Target stackup
- Simplified test method and probing techniques
- Test method tolerant to test fixture variations, imperfections & DUT impedances
- Automation to deal with data explosion
- Material data over all expected environmental conditions

	Topic	Time	Presenter
1	Introduction	9.00 - 9.15	J. Balachandran, Cisco inc
2	PCB Material Characterization Theory	9.15 - 9.45	Ching Chao Huang, Ataitec Corp
3	Modeling Methodology for Accurate Material characterization	9.45 - 10.05	Alvin Wang, Hirose Electricals
4	Addressing Skew Impairments in characterization	10.05-10.20	Clement Luk, Samtec inc
	Break	10.20-10.30	
5	Test fixture design for PCB Methodology	10.30-11.00	Jeremy Baun, Hirose Electricals J. Balachandram, Cisco inc
6	Automation	11.00-11.10	J. Balachandran, Cisco inc
7	Case study & Results	11.10-11.30	Anna Gao, Cisco inc
8	Summary	11.30-11.40	Ching Chao Huang, Ataitec Corp

Outline

- Introduction : J. Balachandran - Cisco inc
- PCB Material Characterization Theory : Ching Chao Huang - AtaiTec Corp
- Modeling PCB Interconnects : Alvin Wang - Hirose Electricals
- Addressing Skew impairments : Clement Luk, Samtec
- Test Fixture Design : Jeremy Baun - Hirose Electricals, J. Balachandran
- Automation : J. Balachandran
- Case Study & Results : Anna Gao – Cisco inc
- Summary : Ching Chao Huang

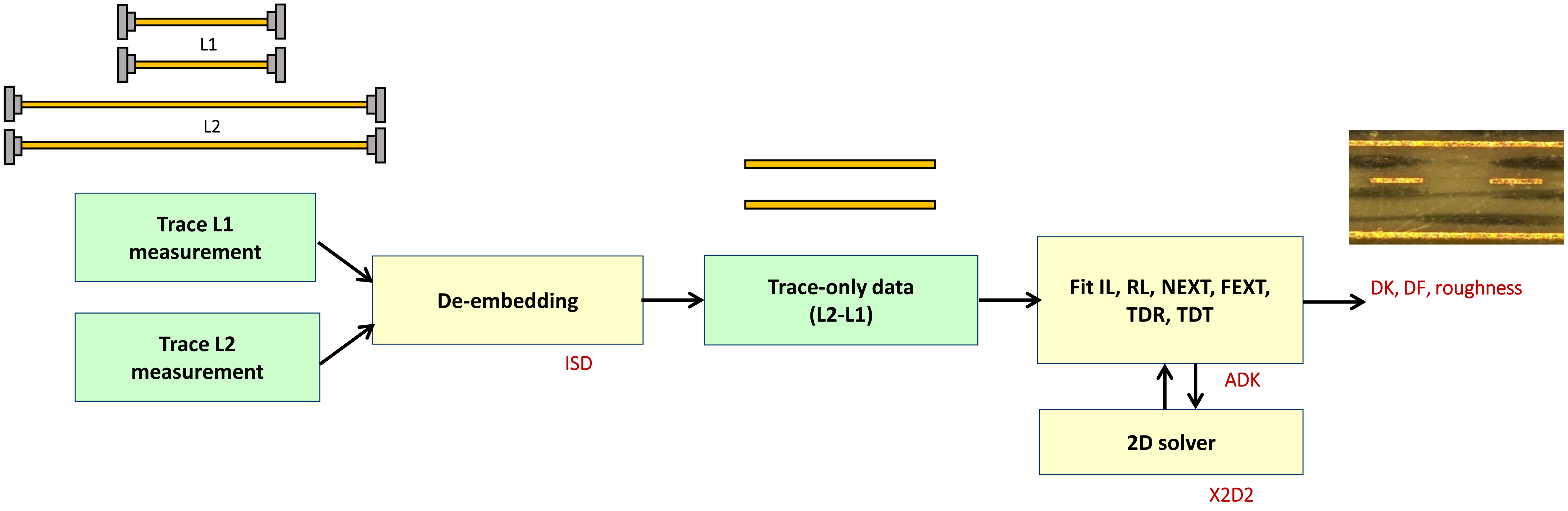
PCB Material Characterization Theory

Outline

- PCB material property extraction flow
- Djordjevic-Sarkar model (for DK/DF)
  - Djordjevic vs. Svensson formats
- Effective conductivity model (for roughness)
  - Conversion from effective conductivity to Huray model
- Templates for 2D solver
- In-Situ De-embedding (ISD)
- Eigenvalue (Delta L) solution
- DK/DF/SR extraction example

PCB material property extraction flow
Self-consistent* MPX methodology

- Measure short and long traces by VNA, de-embed short trace from long trace and match all IL, RL, NEXT, FEXT and TDR/TDT of trace-only data by 2D solver to extract DK, DF and roughness.

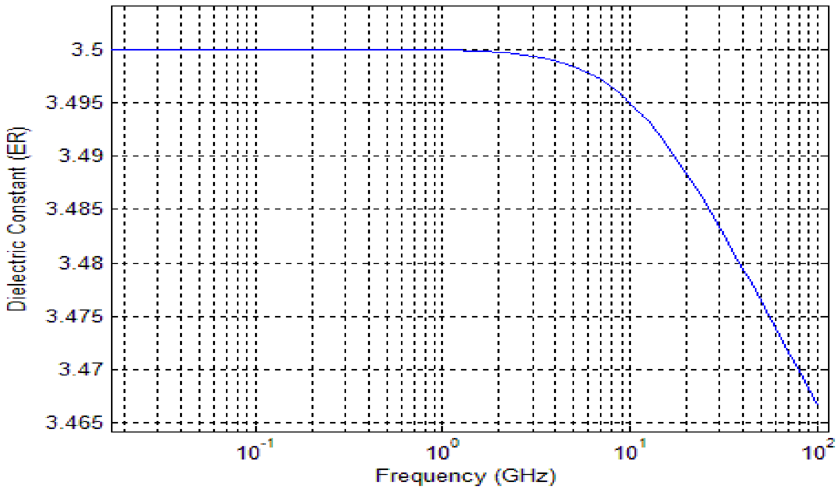


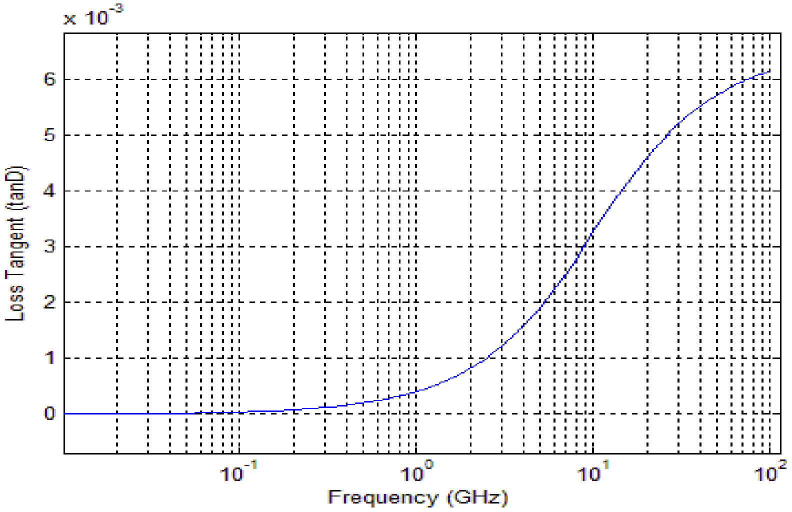
* Built-in verification with extracted models matching all de-embedded data.

Djordjevic-Sarkar model (for DK/DF)

- Need only four variables: ε_∞ , $\Delta\varepsilon$, m_1 , m_2 to represent wide-band DK & DF.

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$





$\varepsilon_\infty = 3.35$, $\Delta\varepsilon = 0.15$, $m_1 = 10$, $m_2 = 14.5$

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Djordjevic and Svensson formats are equivalent.

$$
\begin{aligned}
\varepsilon &= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right) \\
&= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{f_2 + i \cdot f}{f_1 + i \cdot f}\right) \\
&= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{A \cdot e^{i\phi_2}}{B \cdot e^{i\phi_1}}\right) \\
&= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \log_e\left(\frac{A \cdot e^{i\phi_2}}{B \cdot e^{i\phi_1}}\right) \\
&= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \left\{\log_e\left(\frac{A}{B}\right) + i(\phi_2 - \phi_1)\right\} \\
&= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \left\{\frac{1}{2}\log_e\left(\frac{f_2^2 + f^2}{f_1^2 + f^2}\right) + i\left(\tan^{-1}\left(\frac{f}{f_2}\right) - \tan^{-1}\left(\frac{f}{f_1}\right)\right)\right\} \\
&= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \left\{\frac{1}{2}\log_e\left(\frac{\tau_2^2\left(1+\omega^2\tau_1^2\right)}{\tau_1^2\left(1+\omega^2\tau_2^2\right)}\right) + i\left(\tan^{-1}(\omega\tau_1) - \tan^{-1}(\omega\tau_2)\right)\right\} \\
&= \varepsilon_r \cdot (1 - i\tan\delta) \\
&= \varepsilon_r \cdot \left(1 - i\frac{\sigma}{2\pi f \varepsilon_r \varepsilon_0}\right)
\end{aligned}
$$

X2D2* ← $\varepsilon_\infty \quad \Delta\varepsilon \quad m_1 \quad m_2$

* X2D2 is a 2D solver from AtaiTec (www.ataitec.com)

Djordjevic format

Svensson format

HFSS →

$$
\begin{cases}
\varepsilon_r = \varepsilon_\infty + \Delta\varepsilon \cdot \dfrac{1}{m_2 - m_1} \cdot \dfrac{1}{\log_e(10)} \cdot \dfrac{1}{2}\log_e\left(\dfrac{f_2^2 + f^2}{f_1^2 + f^2}\right) \\
\sigma = 2\pi f \cdot \varepsilon_0 \cdot \Delta\varepsilon \cdot \dfrac{1}{m_2 - m_1} \cdot \dfrac{1}{\log_e(10)} \cdot \left(\tan^{-1}\left(\dfrac{f}{f_1}\right) - \tan^{-1}\left(\dfrac{f}{f_2}\right)\right)
\end{cases}
$$

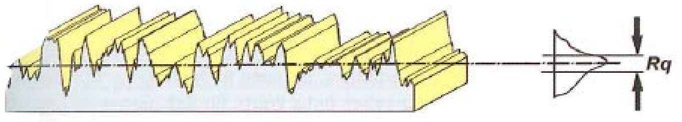
Effective conductivity model (for surface roughness)

- Effective conductivity (by G. Gold & K. Helmreich at DesignCon 2014) needs only two variables: σ_{bulk} , R_q

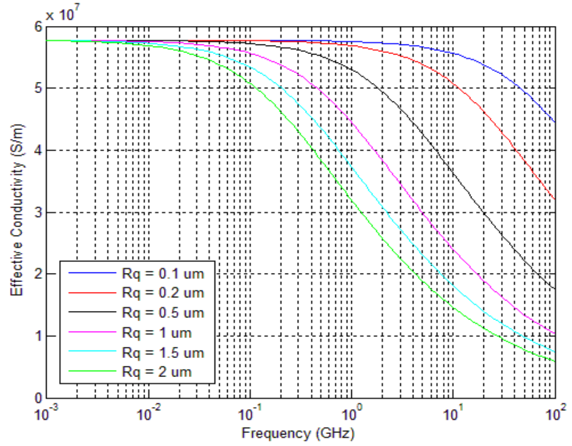
Parameter	Description	Standard
R_q	root mean square	DIN EN ISO 4287
R_a	arithmetic average	DIN EN ISO 4287, ANSI B 46.1
R_k	core roughness depth	DIN EN ISO 13565
R_z	average surface roughness	DIN EN ISO 4287

Table 1: *Statistical parameters to describe surface roughness*

$$\sigma(x)=\sigma_{bulk}\cdot CDF(x)=\sigma_{bulk}\cdot\int_{-\infty}^{x}PDF(x)du=\sigma_{bulk}\cdot\int_{-\infty}^{x}e^{-\frac{u^2}{2R_q^2}}du$$



- Numerically solving $\nabla^2\overline{B}-j\omega\mu\sigma\overline{B}+\frac{\nabla\sigma}{\sigma}\times(\nabla\times\overline{B})=0$ and equating power to that of smooth surface gives σ_{eff}
- A recent paper (by D.N. Grujic in MTT, Nov. 2018) gives closed-form equation.



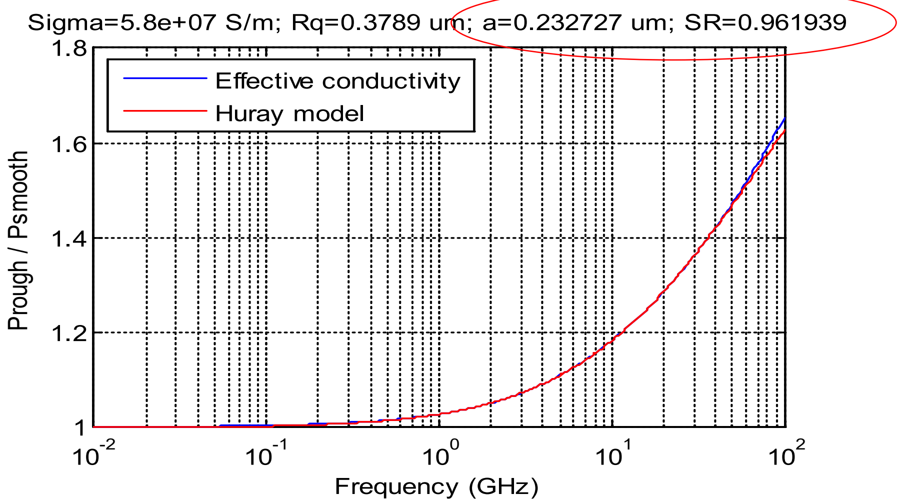
Convert effective conductivity to Huray model

- Huray model

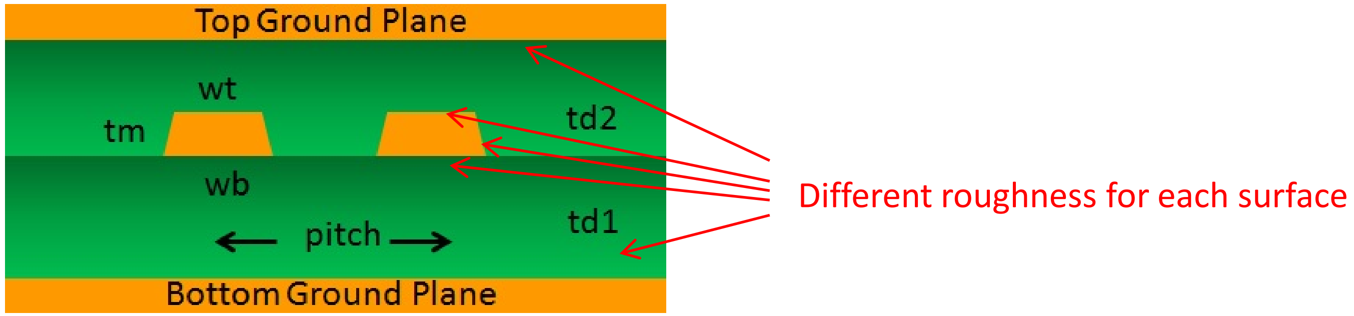
$$\frac{P_{rough}}{P_{smooth}} \approx 1 + \frac{3}{2} \cdot SR \cdot \left(\frac{1}{1 + \frac{\delta(f)}{a} + \frac{1}{2}\left(\frac{\delta(f)}{a}\right)^2} \right)$$

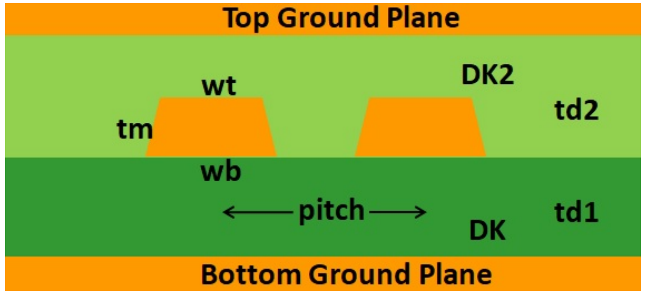
$$\delta(f) = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad ; \quad a = \text{radius} \quad ; \quad SR = \text{surface ratio}$$

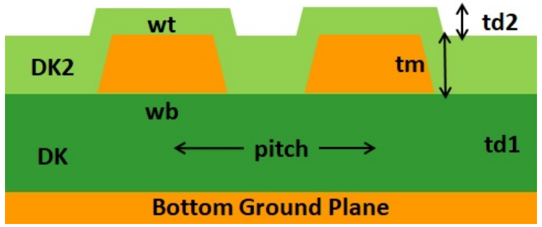
- Curvefit Prough / Psmooth to convert σ_{bulk} , R_q (in X2D2) to a , SR (in HFSS)

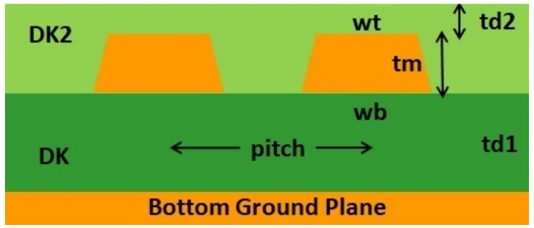


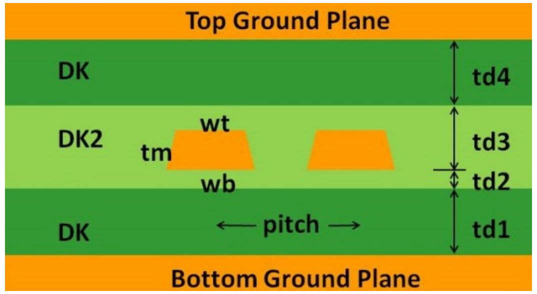
Sample templates for 2D solver

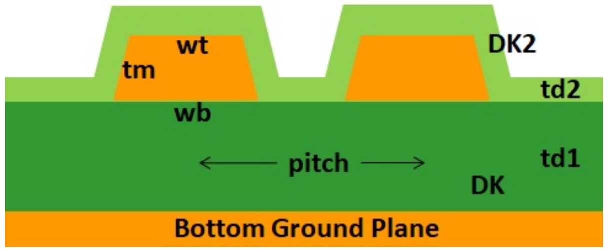


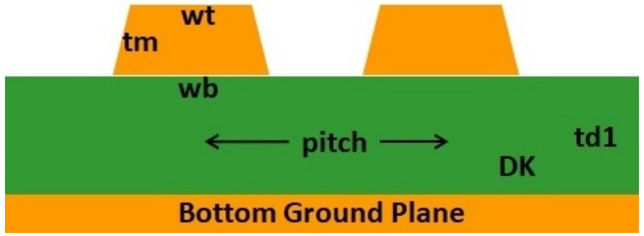






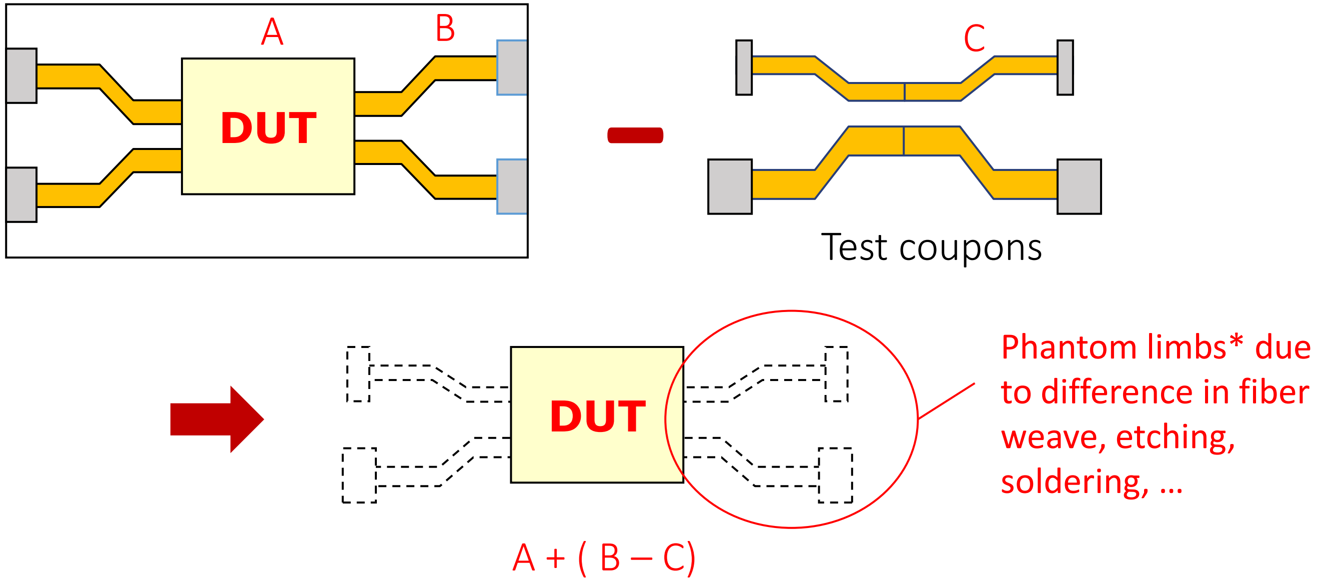






Accurate de-embedding is crucial for DK/DF/SR extraction, but…

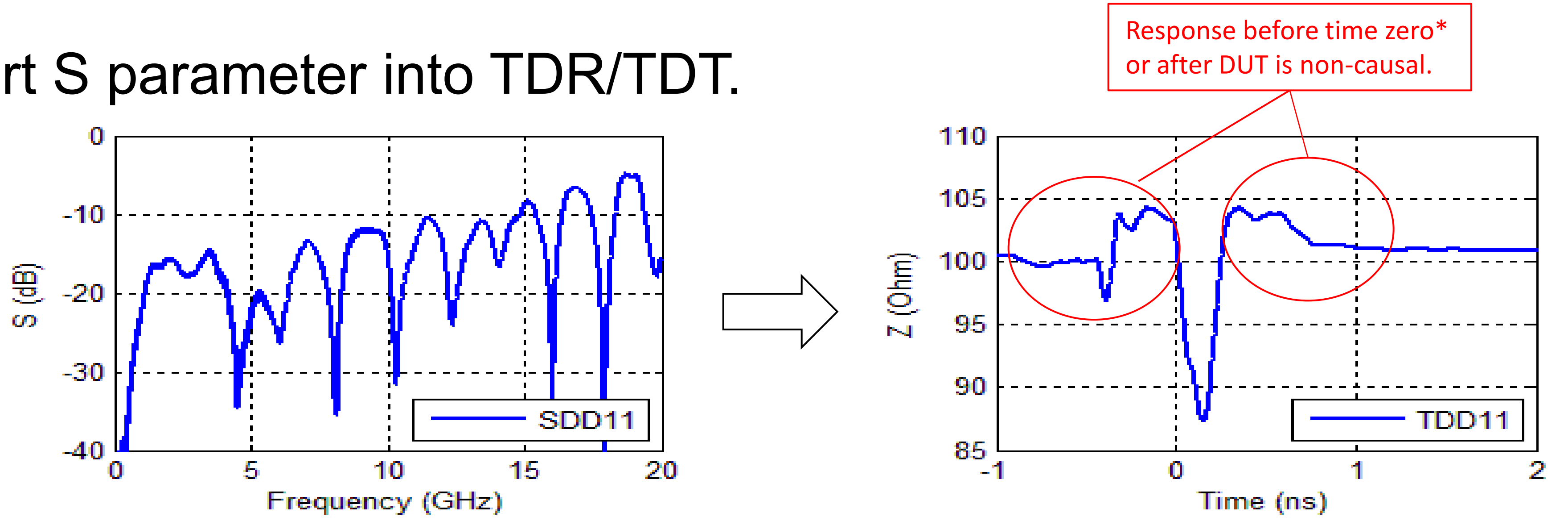
- Many tools use test coupons directly for de-embedding, so difference between actual fixture and test coupons, in the form of causality error, gets piled up into DUT results.



* http://www.edn.com/electronics-blogs/test-voices/4438677/Software-tool-fixes-some-causality-violations by Eric Bogatin

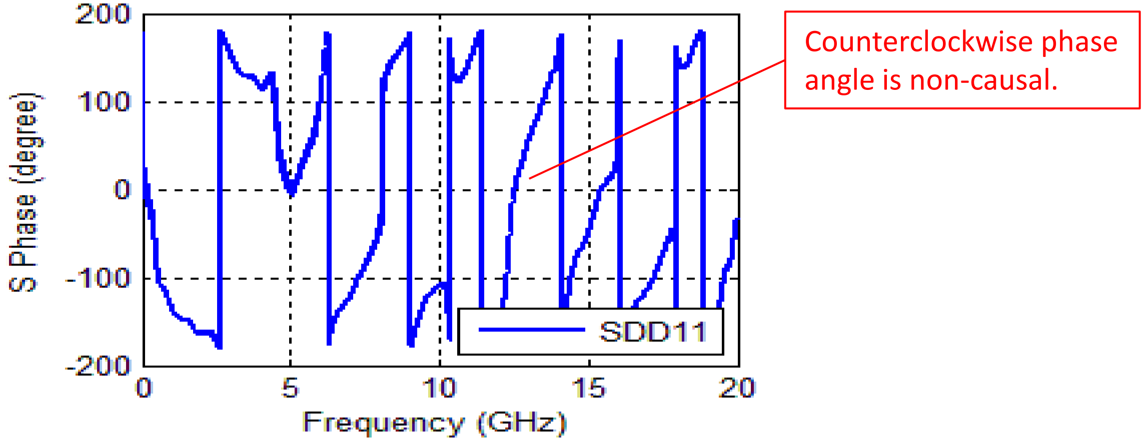
How to identify non-causal S parameter

- Convert S parameter into TDR/TDT.



* Delay waveform by 1ns to see if tools do not show before time zero.

- Check phase angle.



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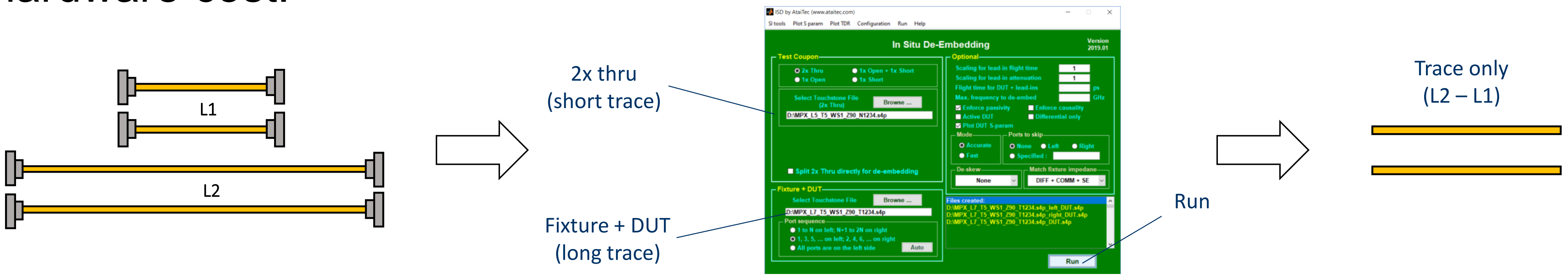
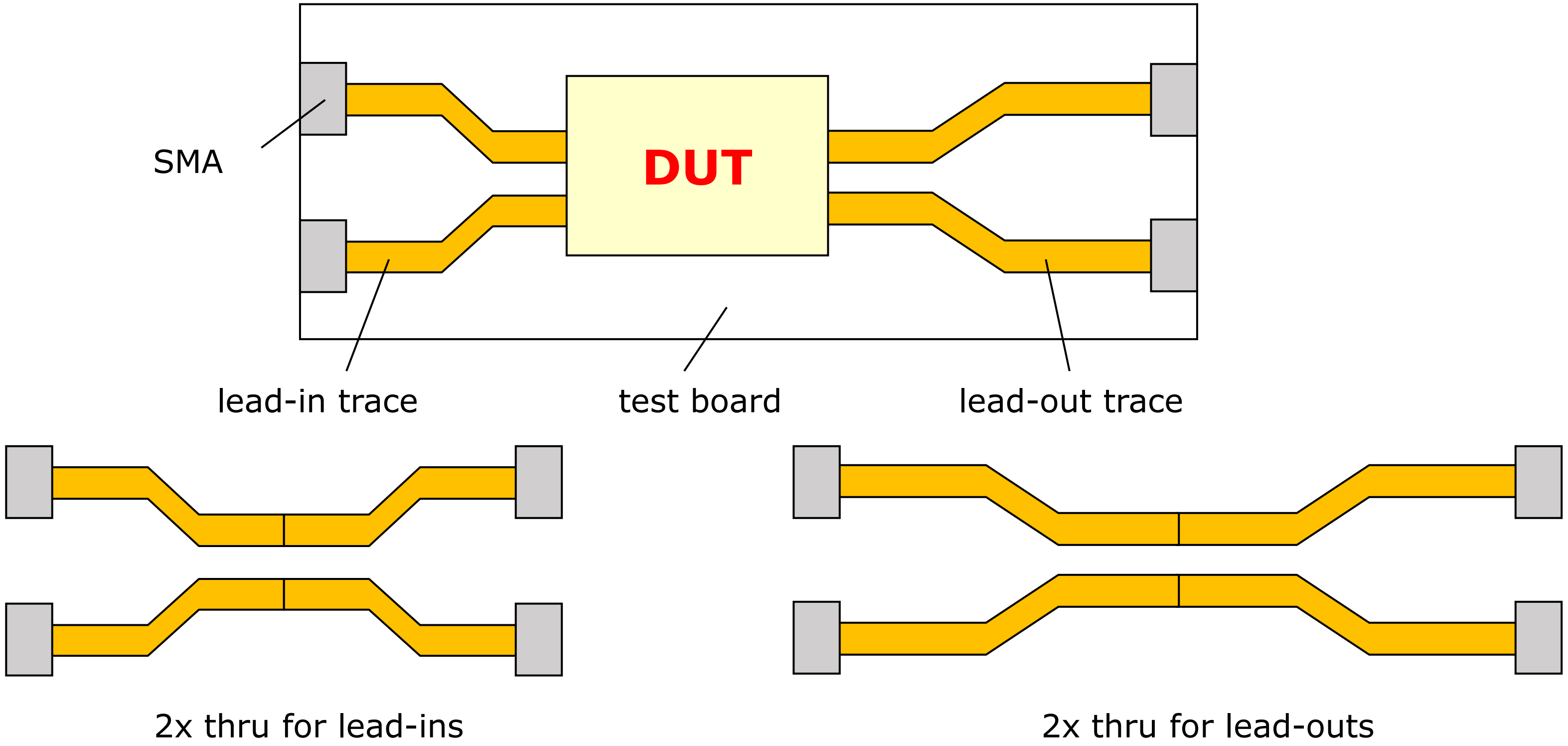
In-Situ De-embedding (ISD)
Introduced to address impedance variation

- ISD uses test coupon (“2x thru” or “1x open / 1x short”) as reference and de-embed fixture’s actual impedance through numerical optimization.
- Other methods use test coupon directly for de-embedding and result in causality error when test coupon and actual fixture to be de-embedded have different impedance.
- ISD addresses impedance variation between test coupon and actual fixture through software, instead of hardware, improving de-embedding accuracy and reducing hardware cost.



What is "2x thru"

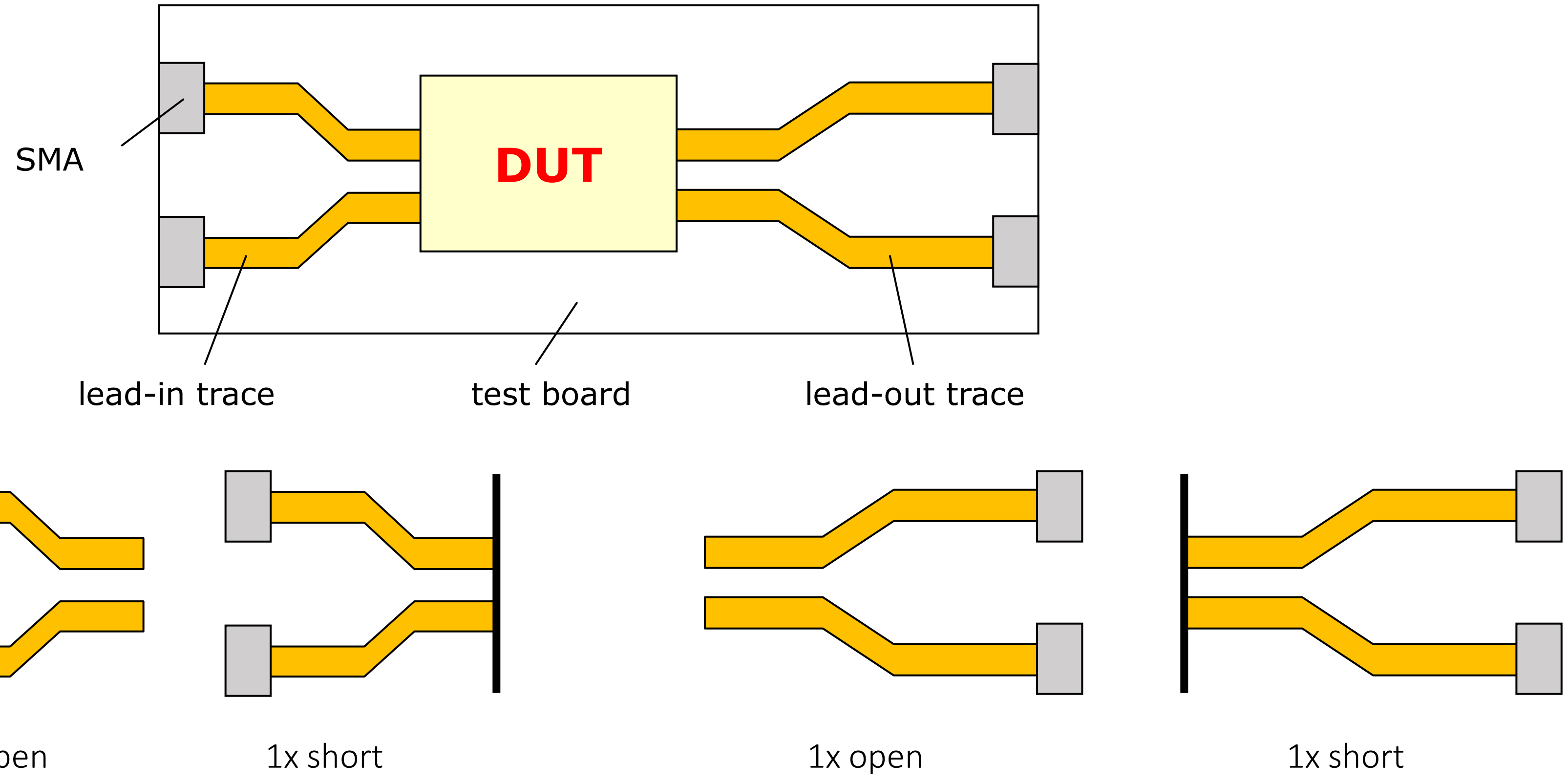
- "2x thru" is 2x lead-ins or lead-outs. For the purpose of DK/DF/SR extraction, "2x thru" corresponds to the shorter trace.



2 sets of "2x thru" are required for asymmetric fixture.

What is "1x open / 1x short"

- "1x open / 1x short" is useful when "2x thru" is not possible (e.g., connector vias, package, …).



Example 1: IEEE P370 plug and play kit
Use 45 ohm 2x thru to de-embed 50 ohm fixture

M11

2x thru

exp 3.2.1 (45 ohm)

exp 3.2.2 (45 ohm)

1.85mm M/M + M/F Adapter

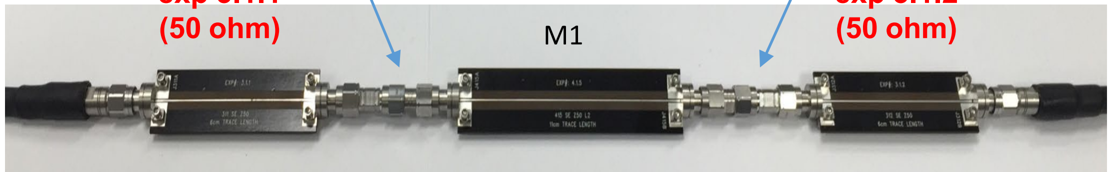
1.85mm M/M + M/F Adapter

M16

exp 3.1.1 (50 ohm)

M1

exp 3.1.2 (50 ohm)

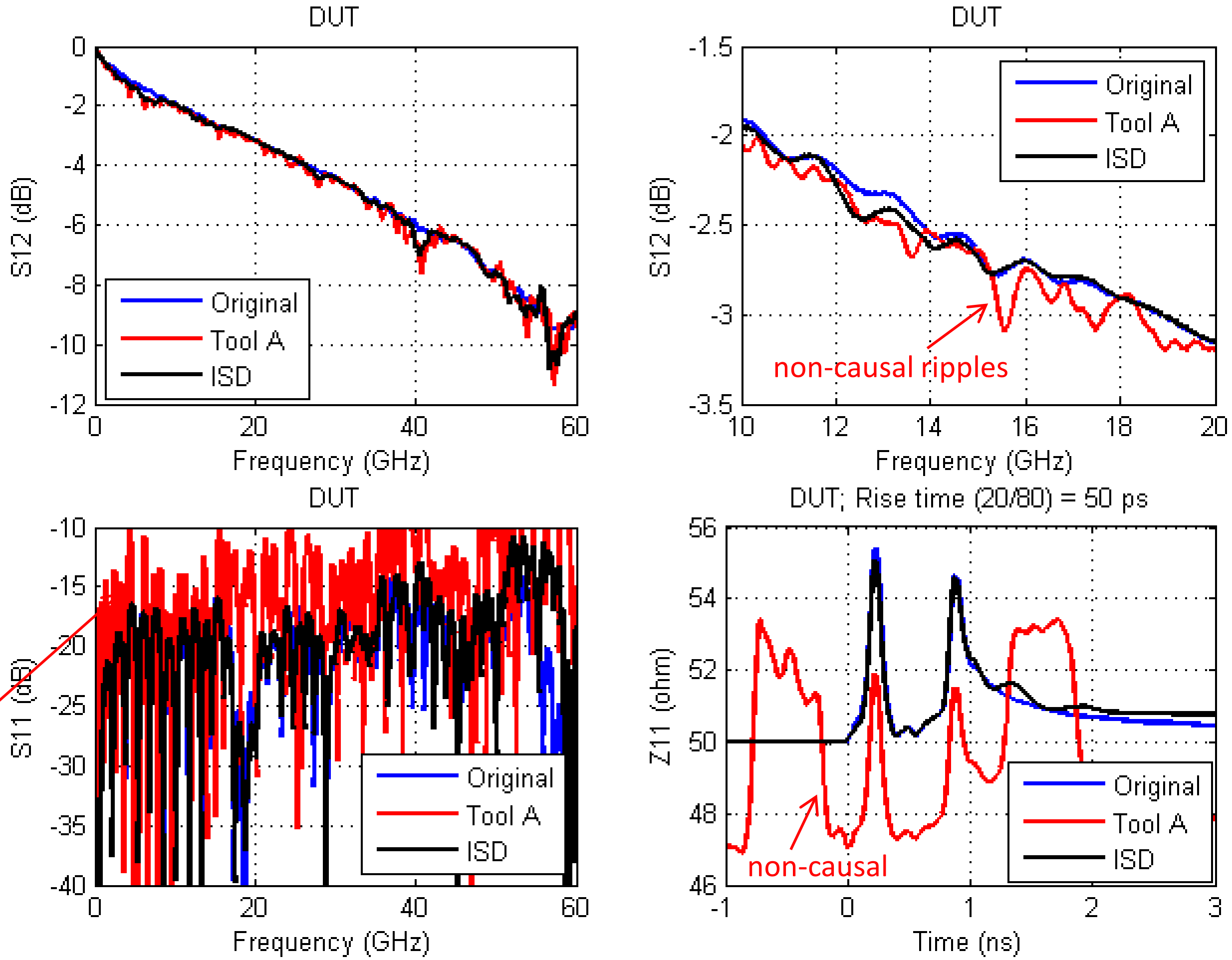


FIXTURE A

exp 4.1.1 6 cm microstrip (DUT)

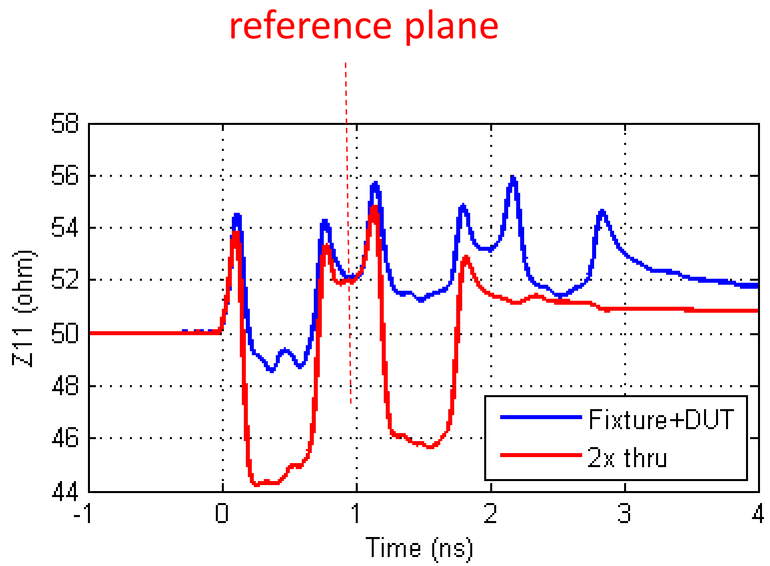
FIXTURE B

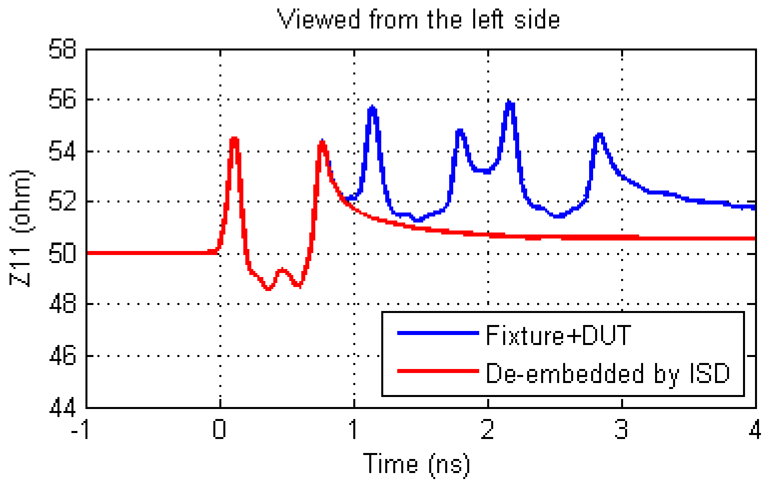
Inaccurate RL is not suitable for DK/DF/SR extraction.



How did ISD do it?

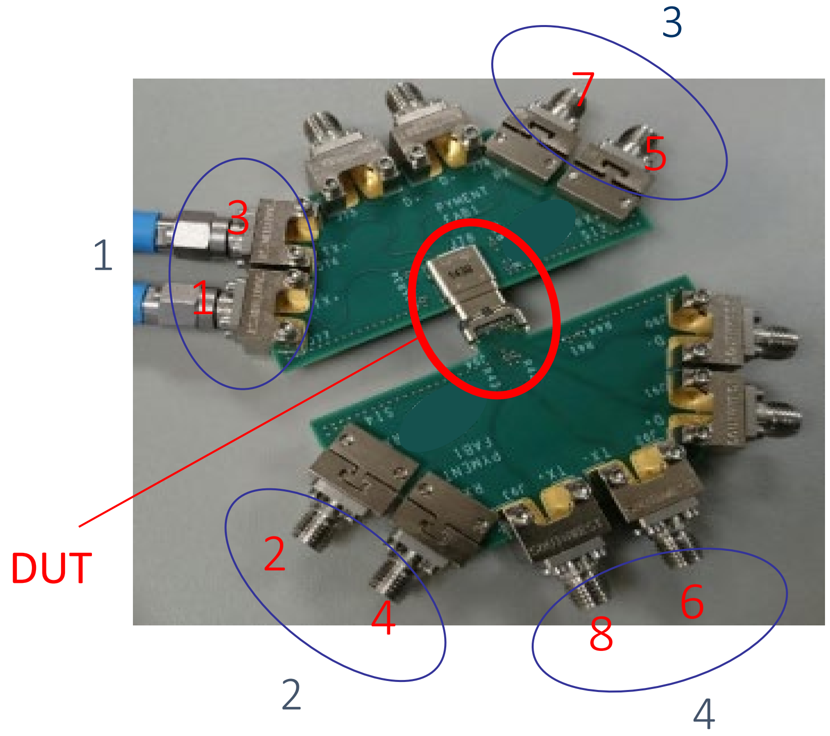
- Through numerical optimization, ISD de-embeds fixture's impedance exactly, independent of 2x thru's impedance

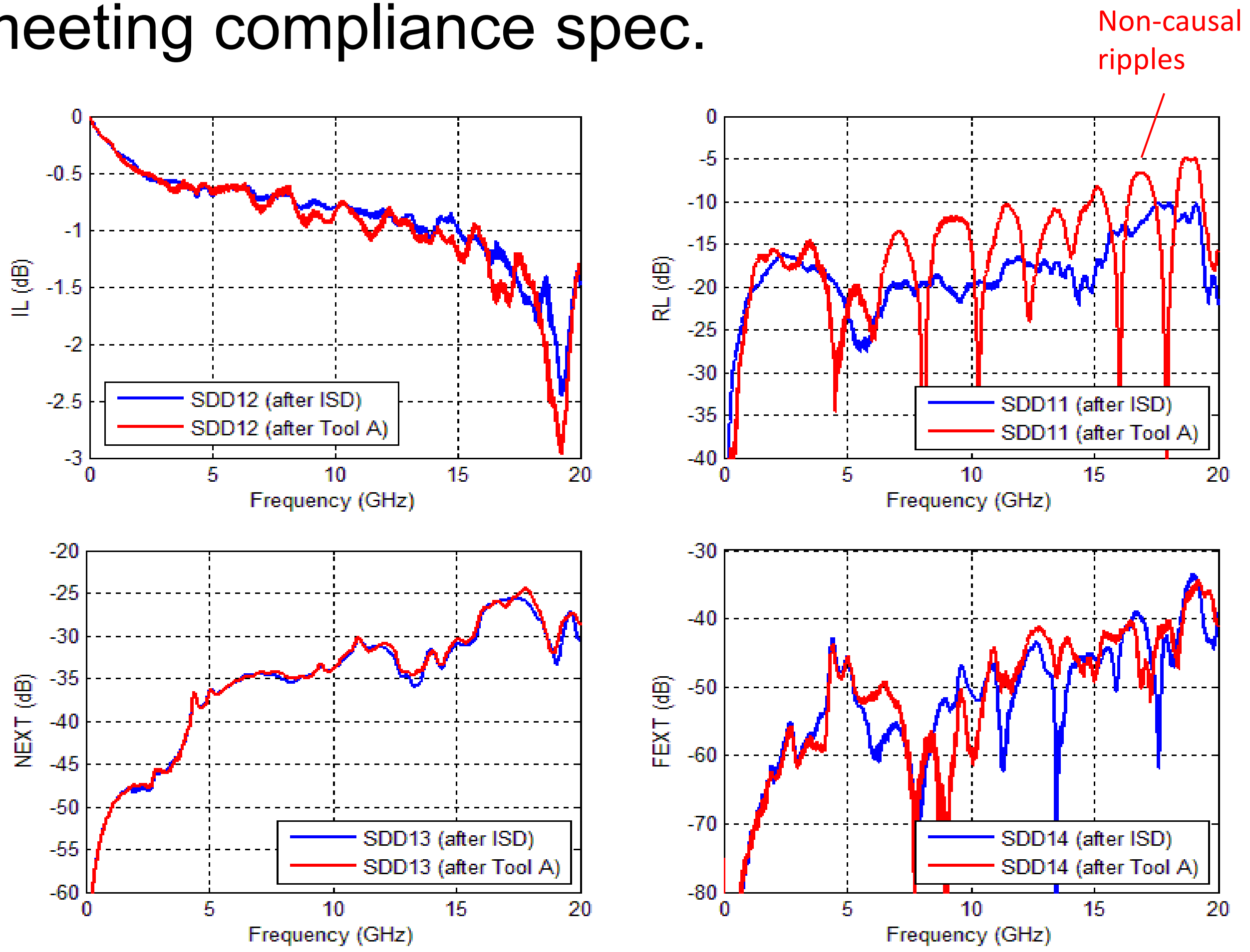




Example 2: USB type C mated connector ISD vs. Tool A

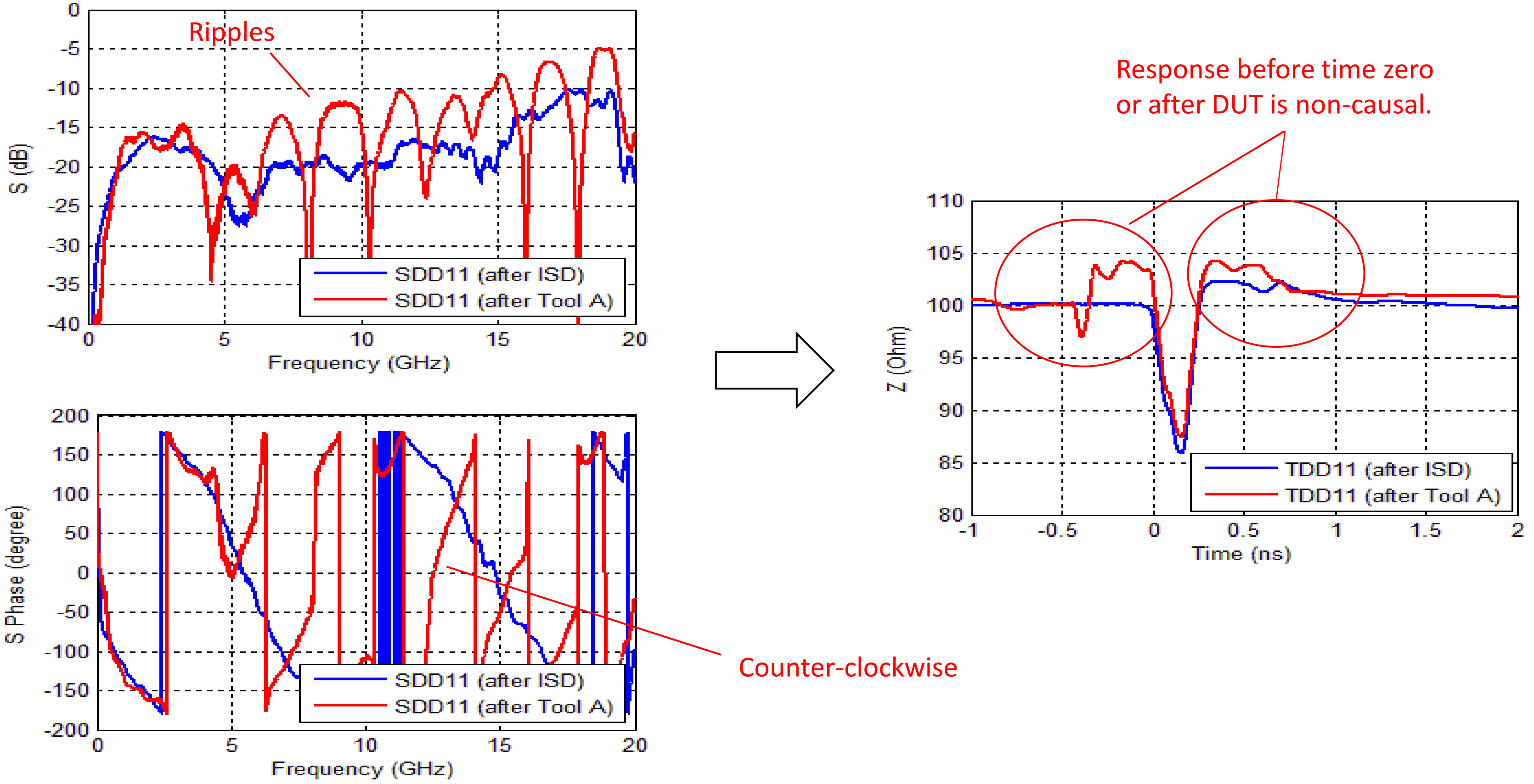
- Good de-embedding is crucial for meeting compliance spec.





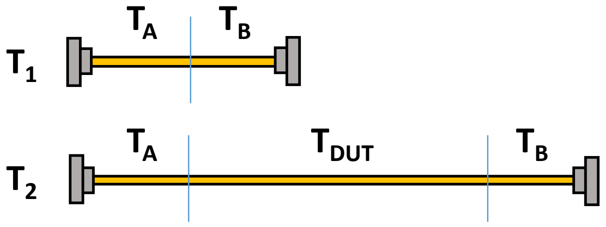
Converting S parameter into TDR/TDT reveals non-causality

- Counter-clockwise phase angle is another indication of non-causality.



Eigenvalue (Delta L) solution: not de-embedding
For calculating trace attenuation only

- Convert S to T for short and long trace structures
- Assume the left (and right) sides of short and long trace structures are identical
- Assume DUT is uniform transmission line
- Trace-only attenuation is written in one equation.



$$T_1 = T_A \cdot T_B$$

$$T_2 = T_A \cdot T_{DUT} \cdot T_B$$

$$\Rightarrow \quad T_2 \cdot T_1^{-1} = T_A \cdot T_{DUT} \cdot T_A^{-1}$$

For uniform transmission line:

$$T_{DUT} = P \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{pmatrix} \cdot P^{-1}$$

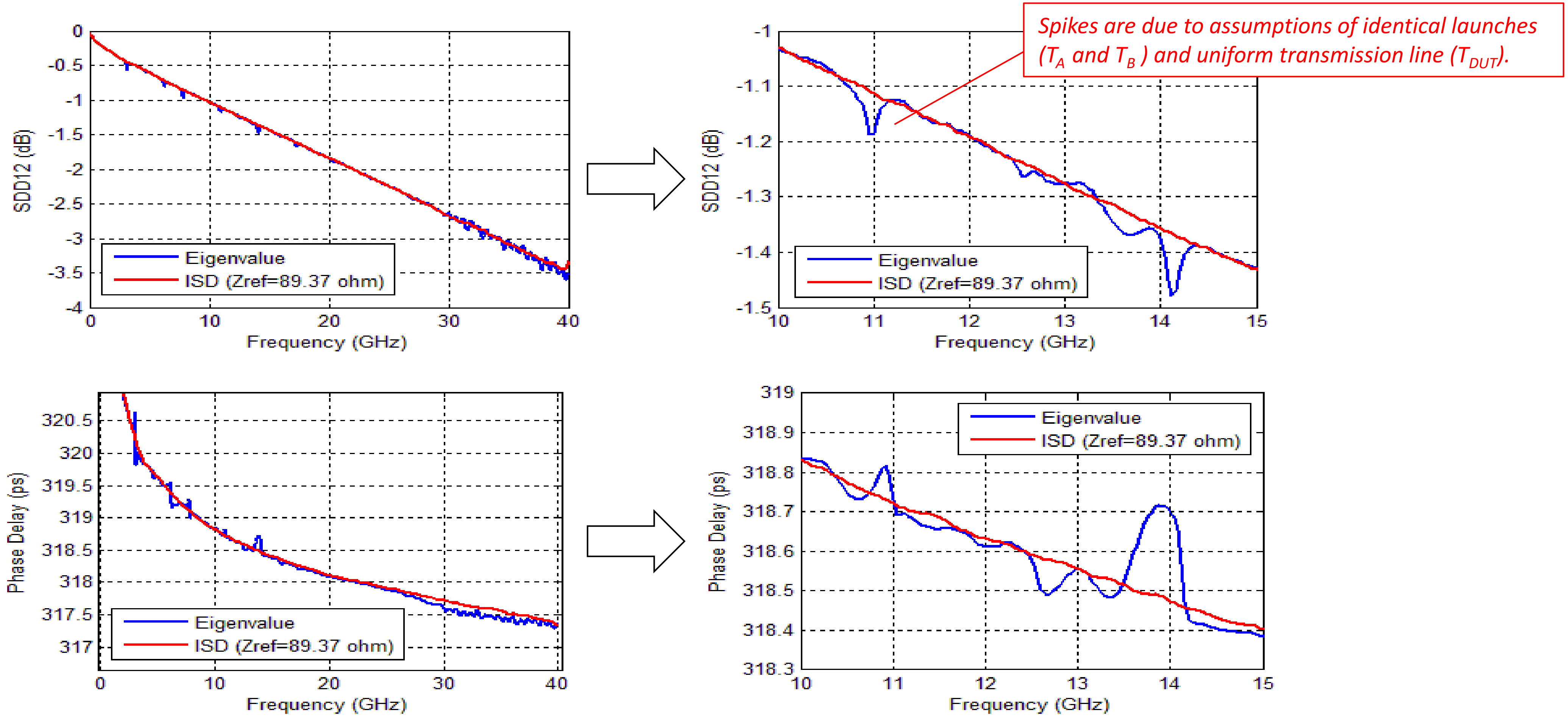
Let $T_2 \cdot T_1^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix}$

$$\Rightarrow \quad e^{-\gamma l} = \frac{(a+d) \pm \sqrt{(a-d)^2 + 4bc}}{2}$$

eigenvalue

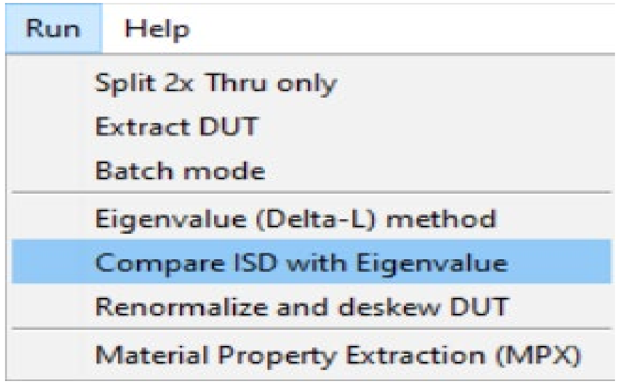
modal propagation constant

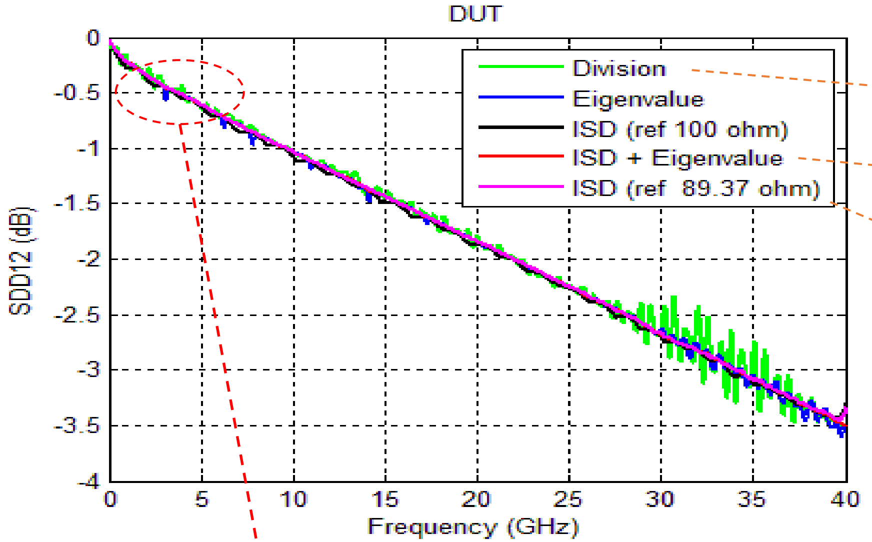
Example 3: 2” (=7”-5”) trace attenuation
Eigenvalue solution is prone to spikes



ISD’s spike-free results help DK/DF/SR extraction later.

ISD vs. eigenvalue solution

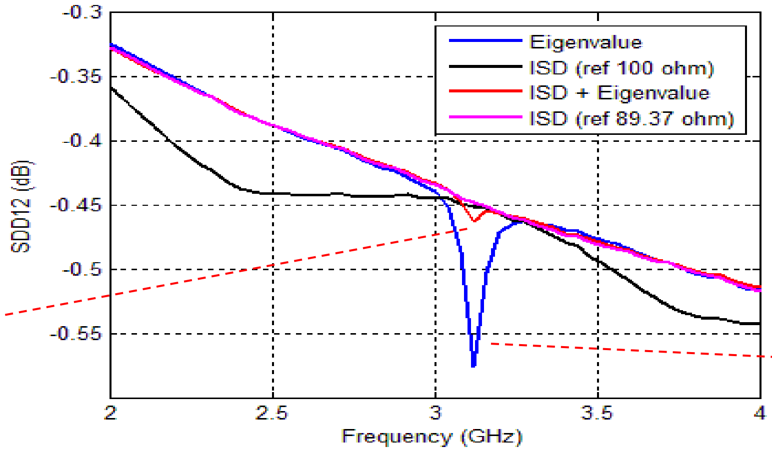




Direct dB subtraction

Eigenvalue of ISD results

Renormalize ISD results
by trace impedance
(automatically calculated)

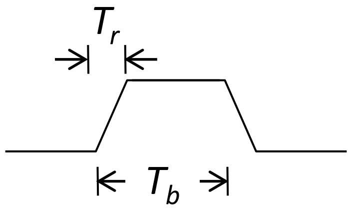


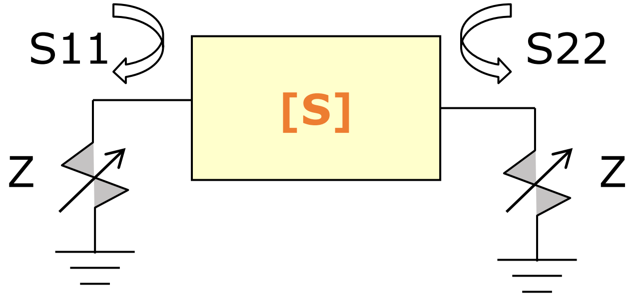
Spikes are due to assumption of uniform transmission line (T_{DUT}).

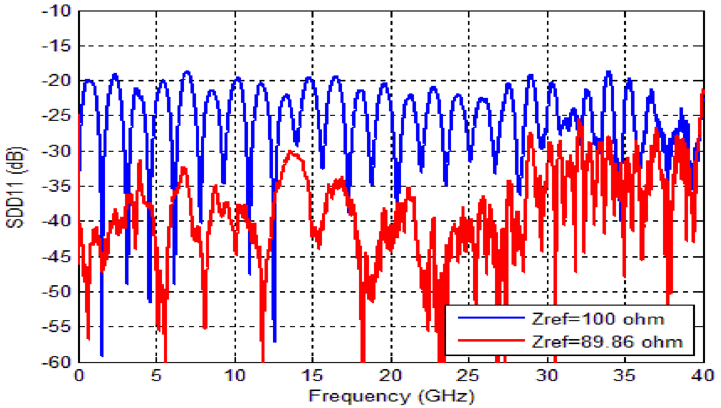
Spikes are due to assumptions of identical launches (T_A and T_B) and uniform transmission line (T_{DUT}).

Define impedance by minimal RL

- Vary reference impedance Z until reflected energy is minimal.



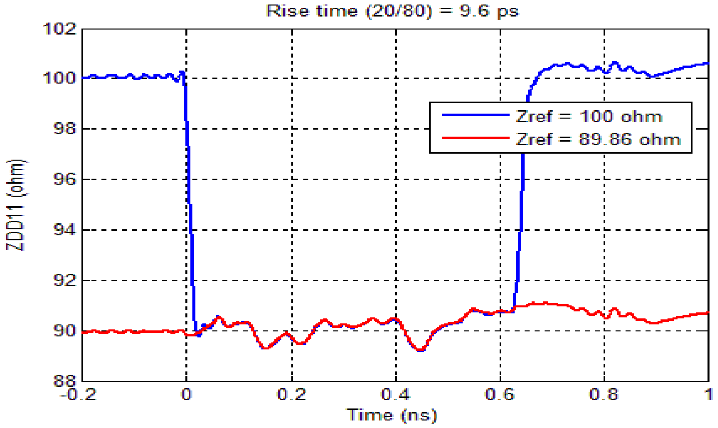




Minimize:

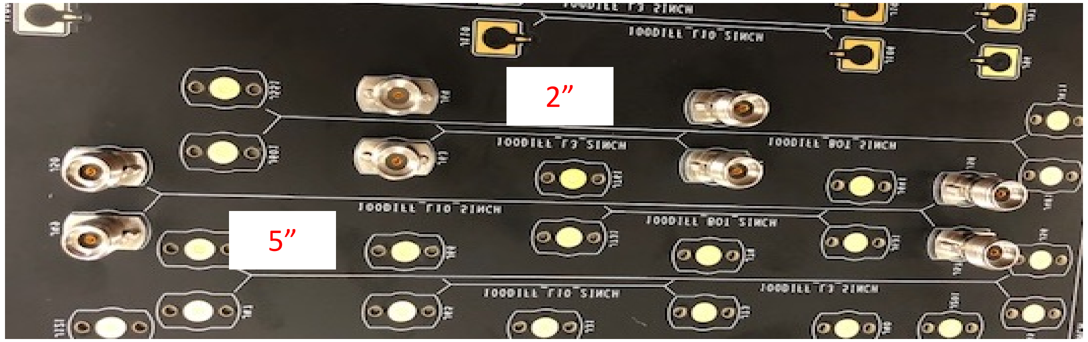
$$\varphi = \int_{f_{\min}}^{f_{\max}} \left\{ \left|S_{11}(f)\right|^2 + \left|S_{22}(f)\right|^2 \right\} \cdot \left|w(f)\right|^2 df$$

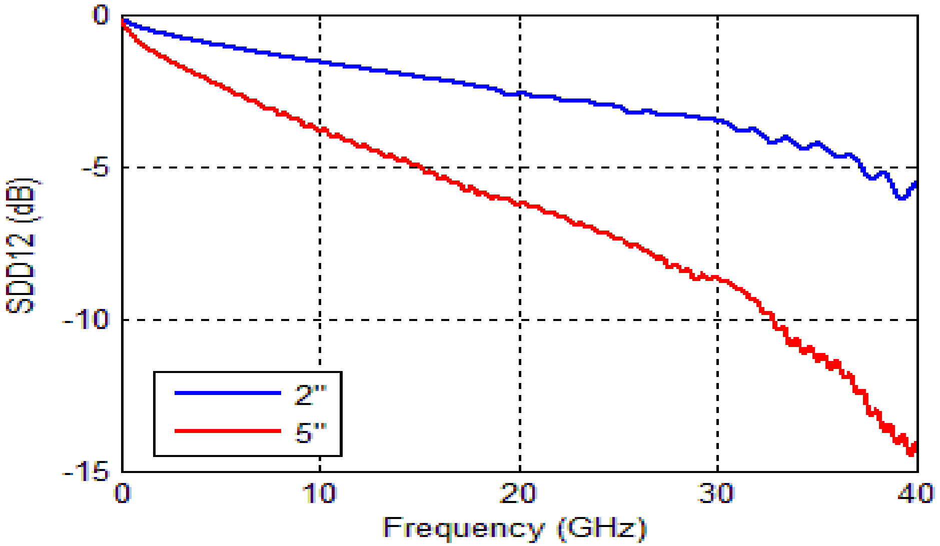
$$w(f) = \frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}$$

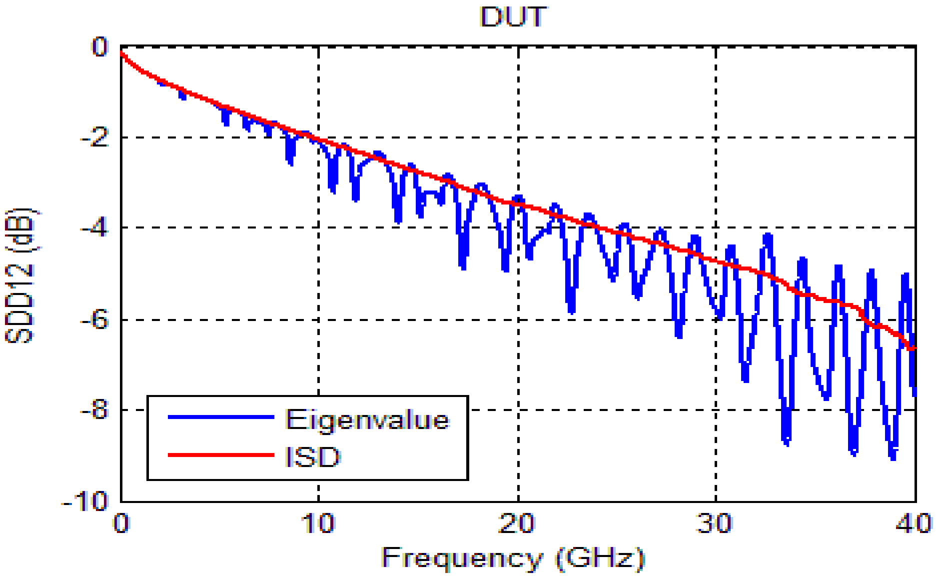


T_b=40ps
T_r=16ps

Example 4: Eigenvalue solution becomes unstable in this case, but why?

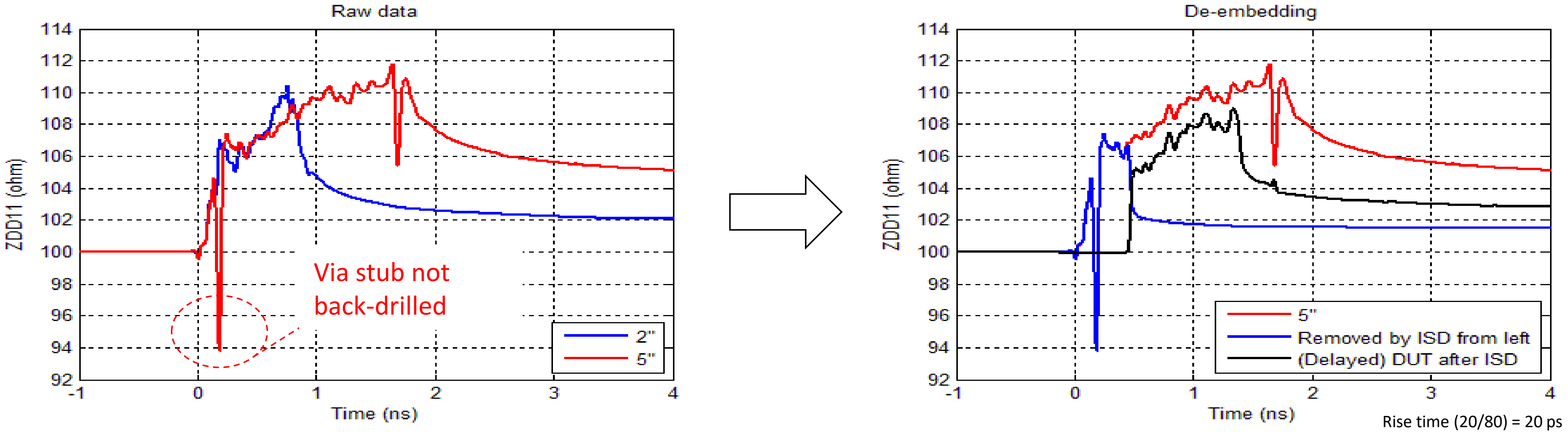






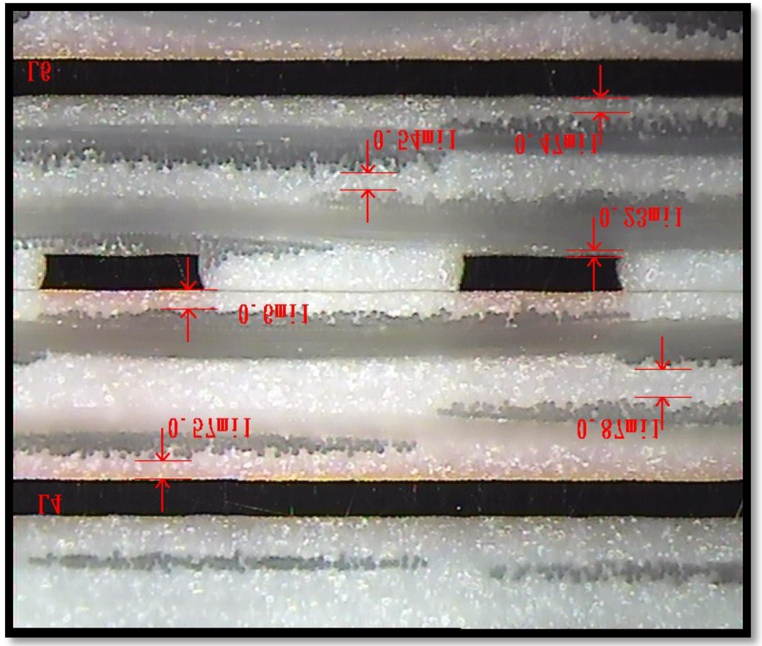
TDR of raw data reveals why…
2” structure was back-drilled but 5” was not

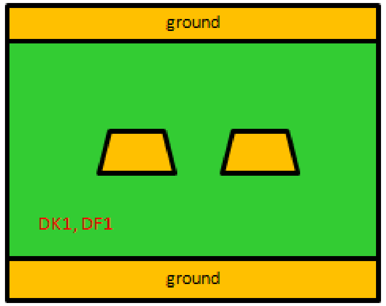
- Eigenvalue solution assumes 2” and 5” structures have identical launches.
- ISD de-embeds 5” structure’s launch correctly.



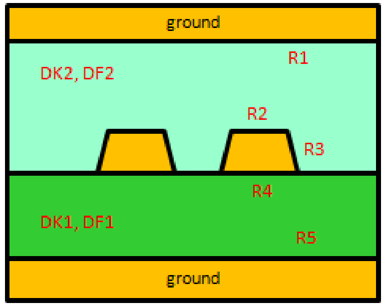
DK/DF/SR extraction example (7” – 5”)

Optimized variables:
DK1, DF1, DK2, DF2
R1, R2, R3, R4, R5 (roughness)
Metal width and spacing

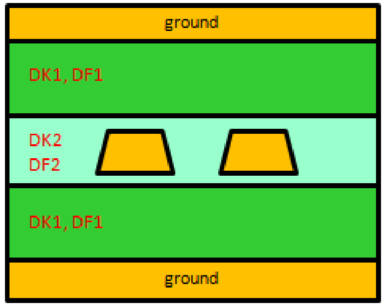




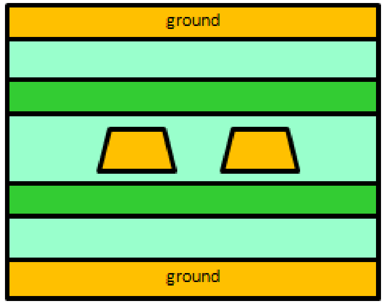
Model 1



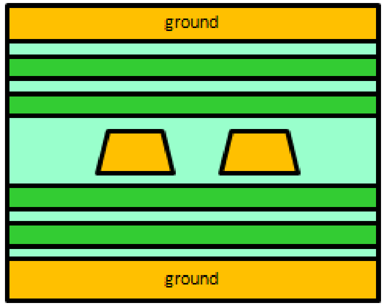
Model 2



Model 3

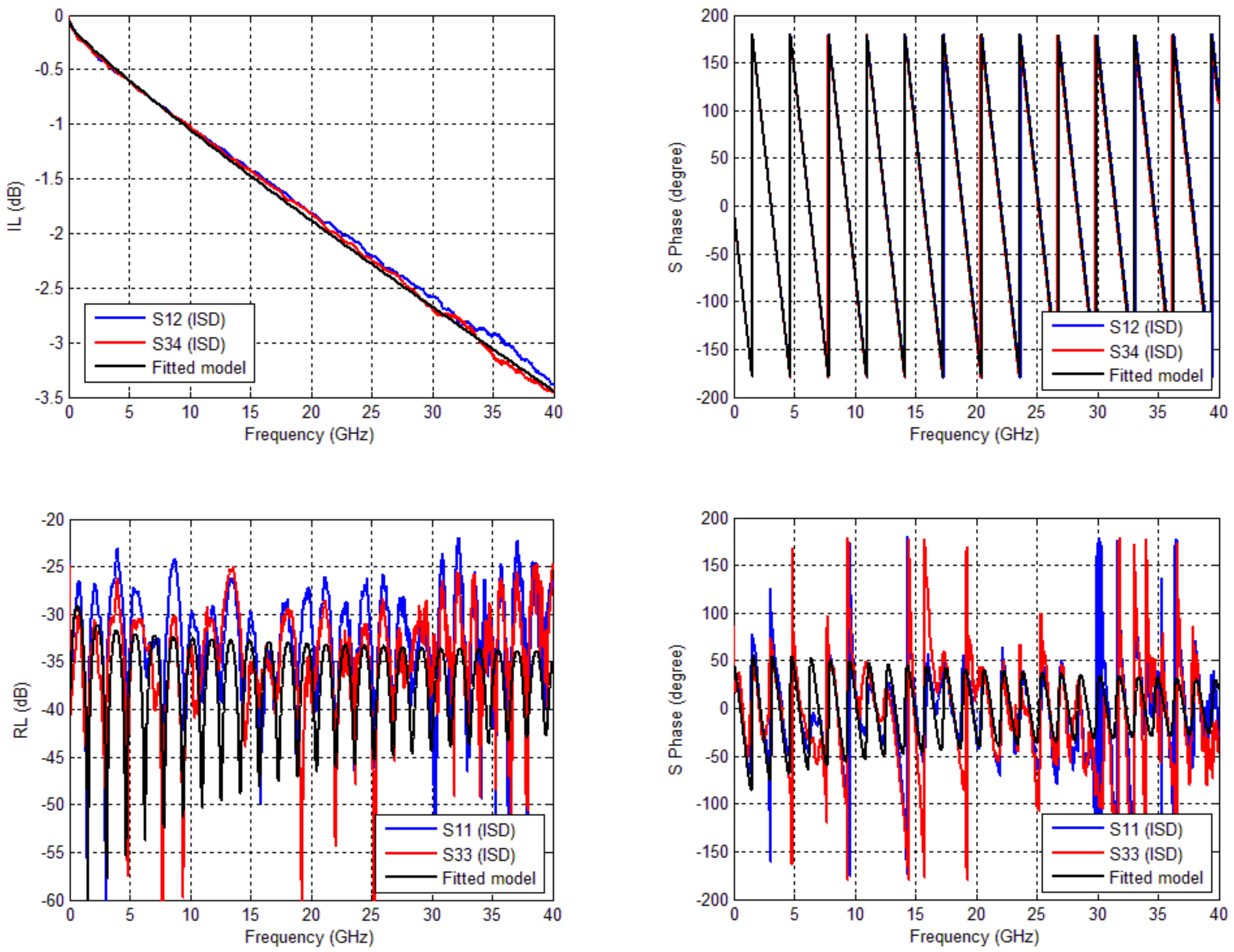


Model 4



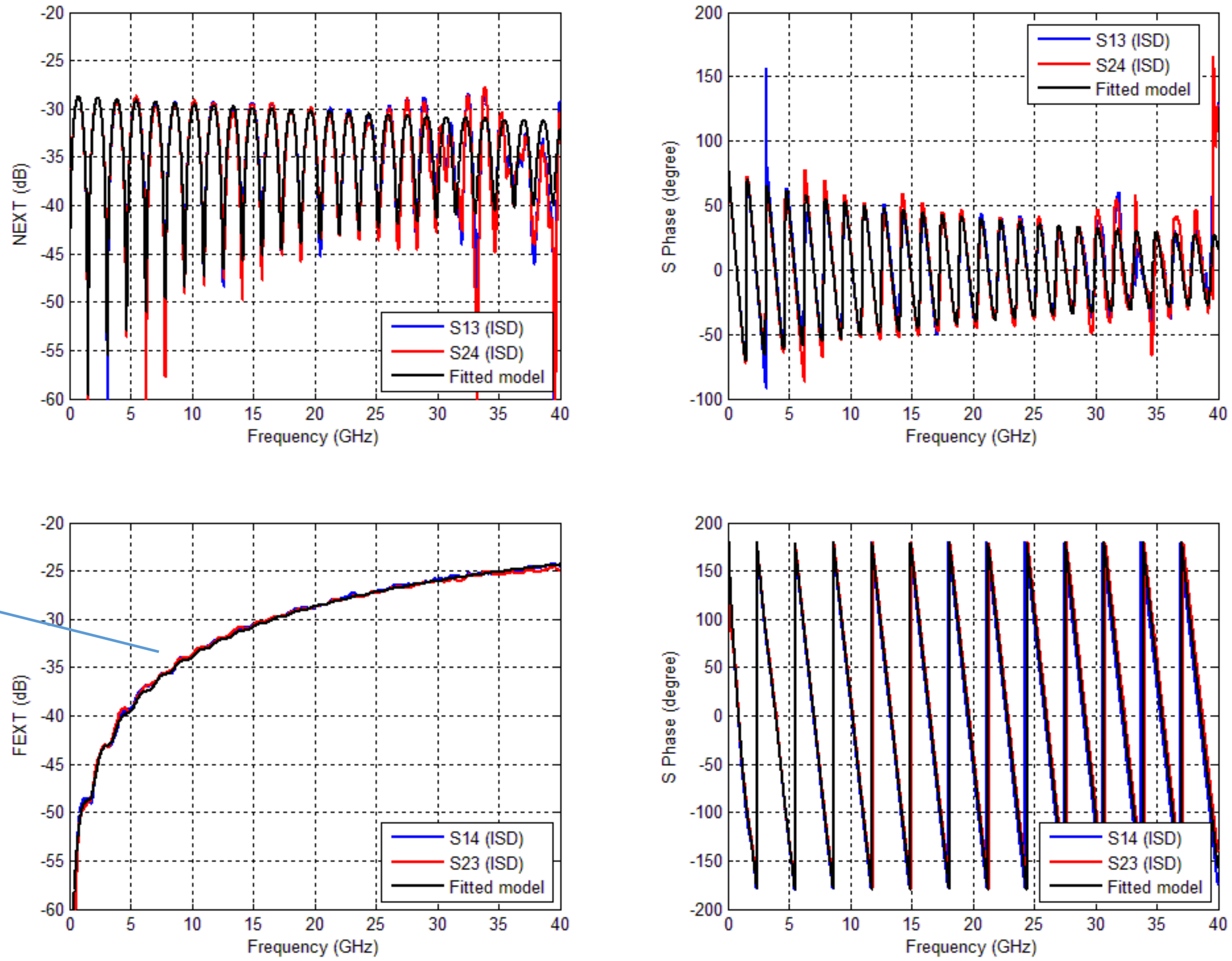
Model 5

Matching IL and RL

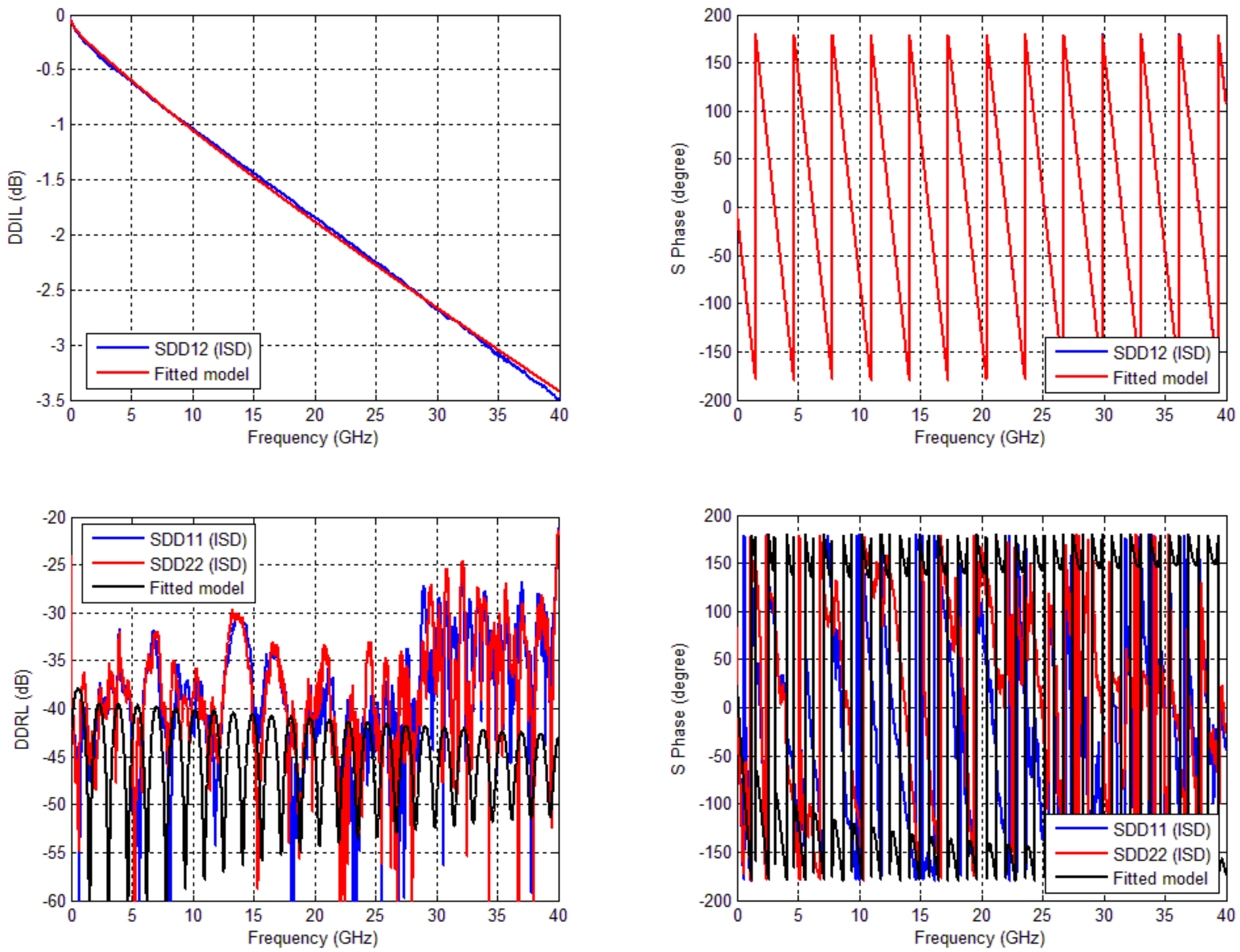


Matching NEXT and FEXT

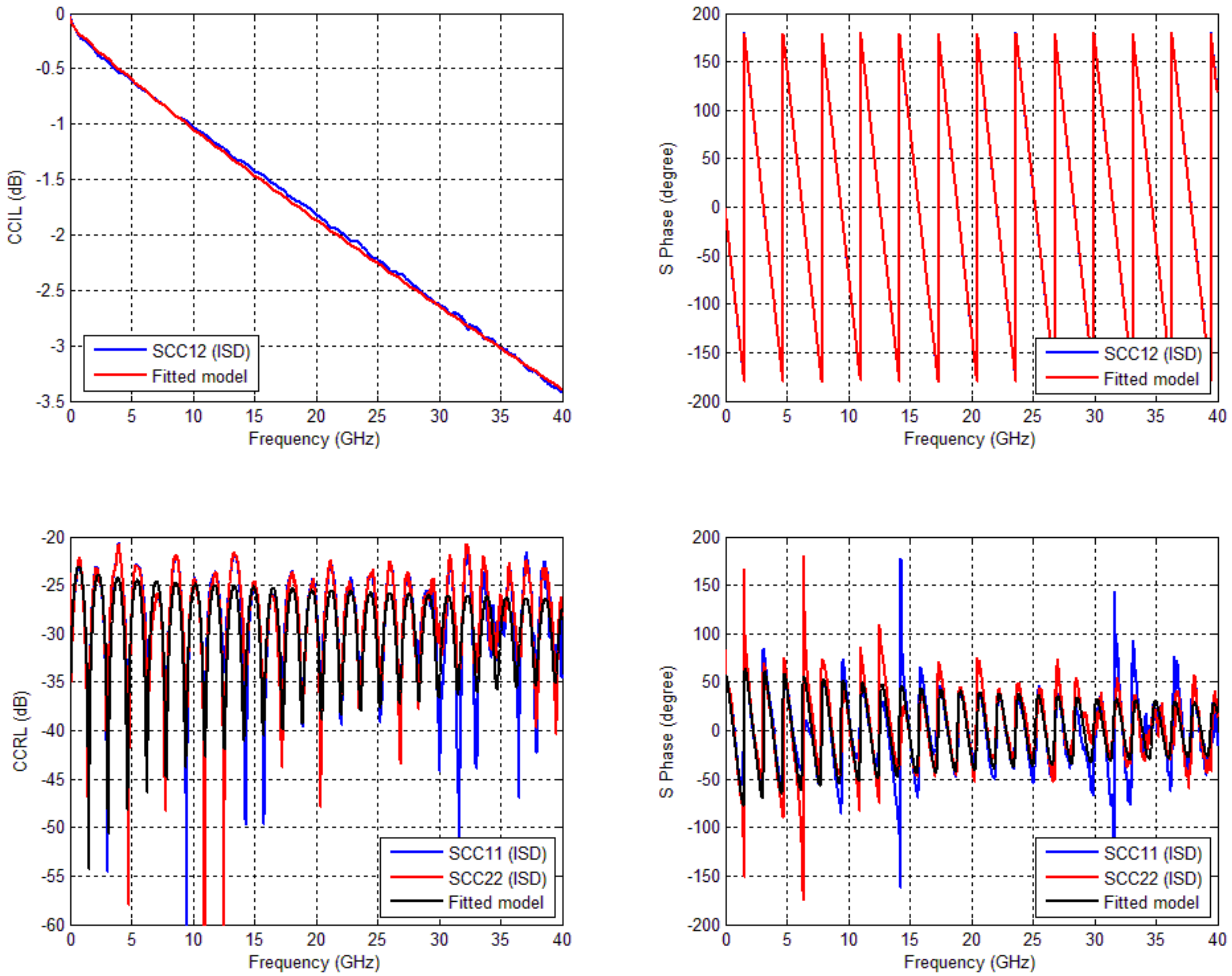
Large FEXT implies inhomogeneous dielectric



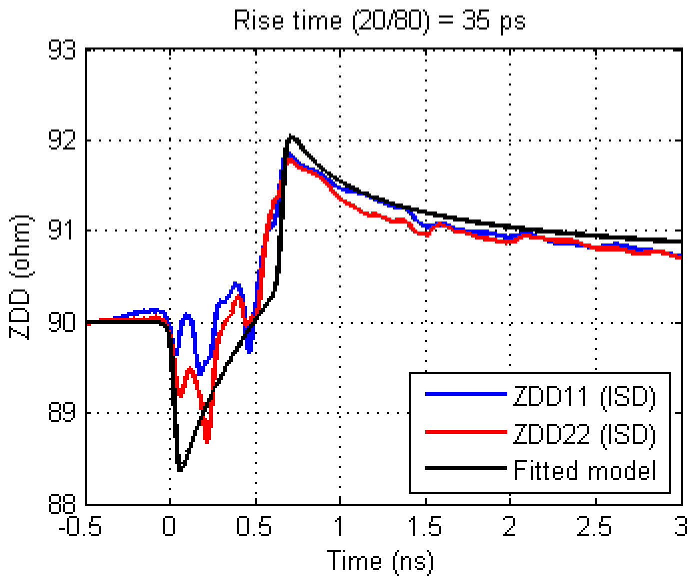
Matching DDIL and DDRL



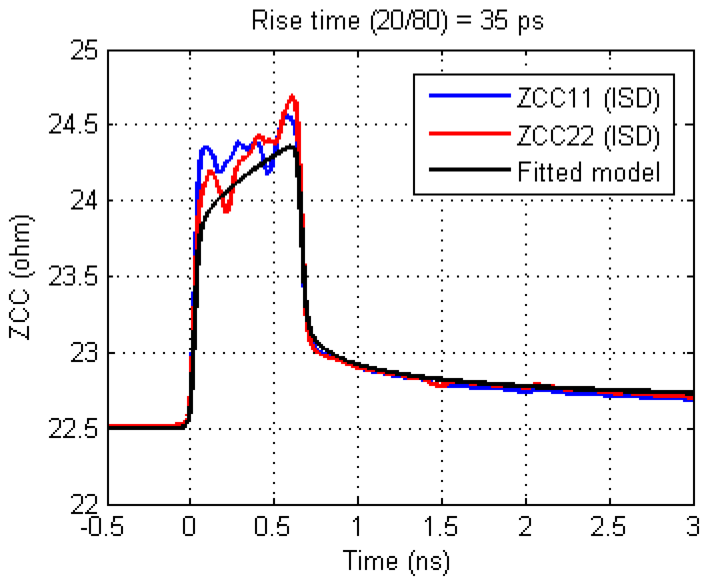
Matching CCIL and CCRL



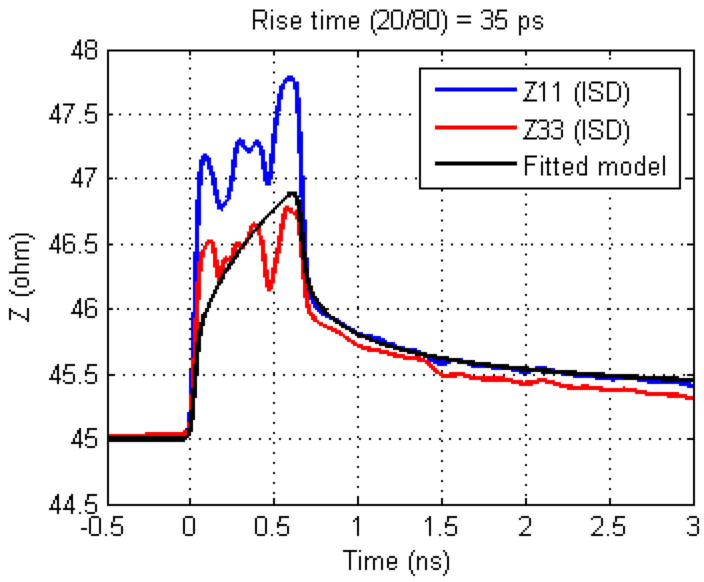
Matching TDR



Differential



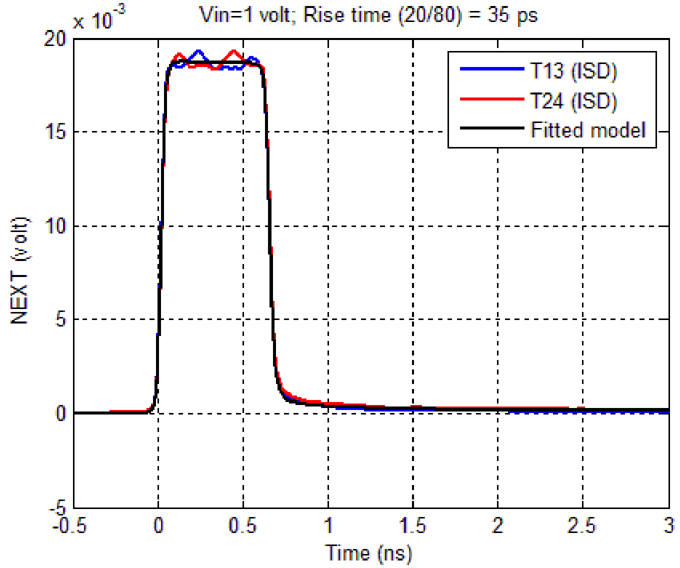
Common



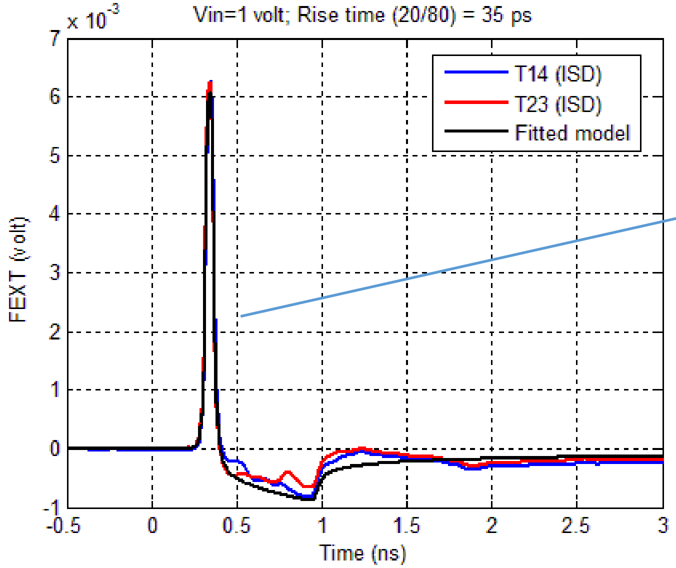
Single-ended

DesignCon 2019 WHERE THE CHIP MEETS THE BOARD

Matching TDT



NEXT

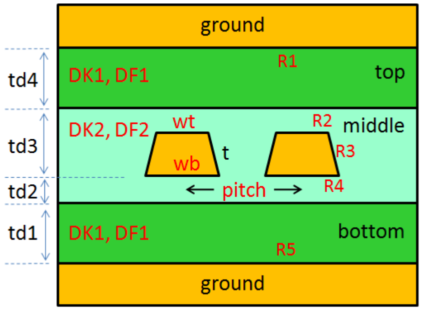


FEXT

Positive polarity implies $K_C > K_L$

DesignCon 2019 WHERE THE CHIP MEETS THE BOARD

Extracted DK1, DF1



$$\varepsilon_\infty = 3.27929$$

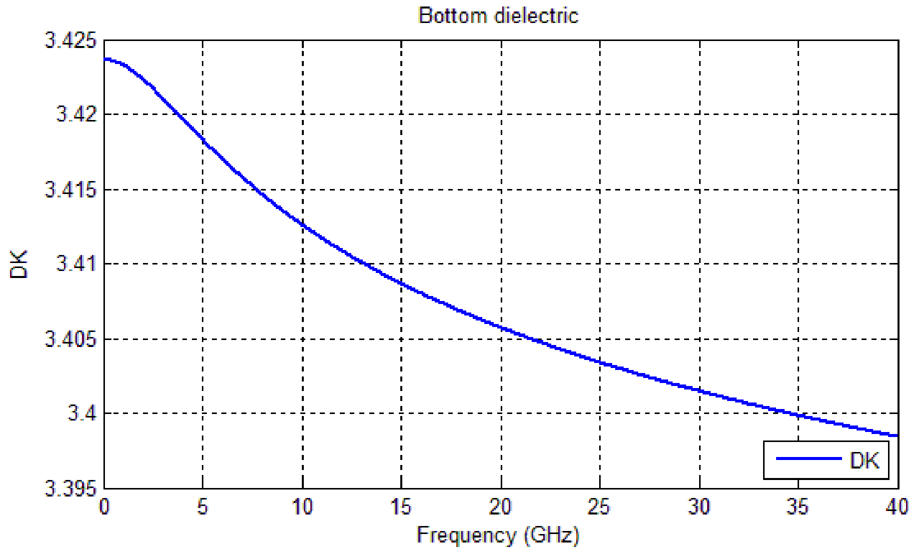
$$\Delta\varepsilon = 0.144348$$

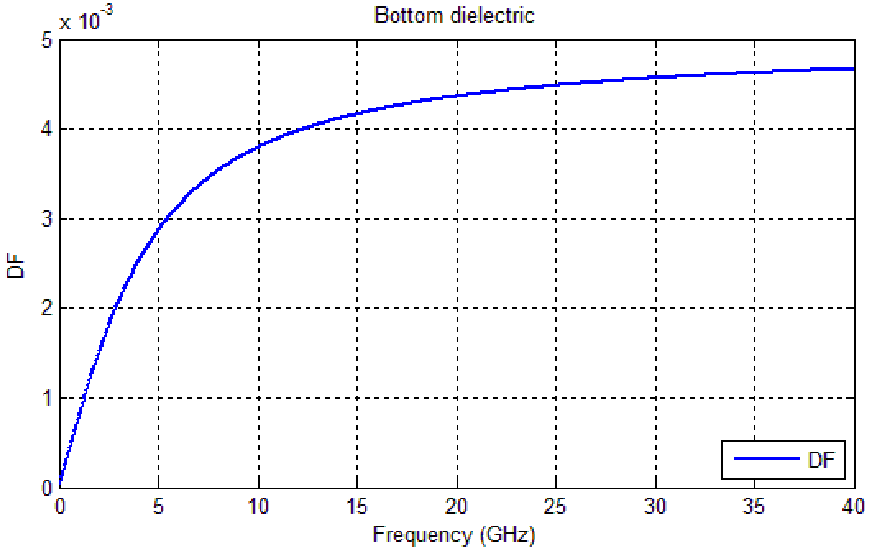
$$m1 = 9.58619$$

$$m2 = 15.4109$$

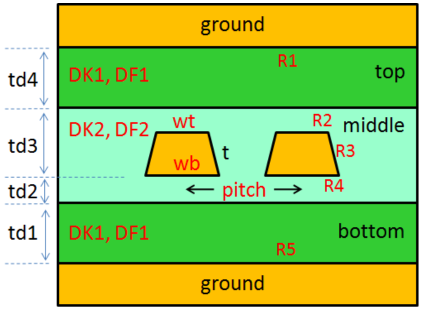
$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$

$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$



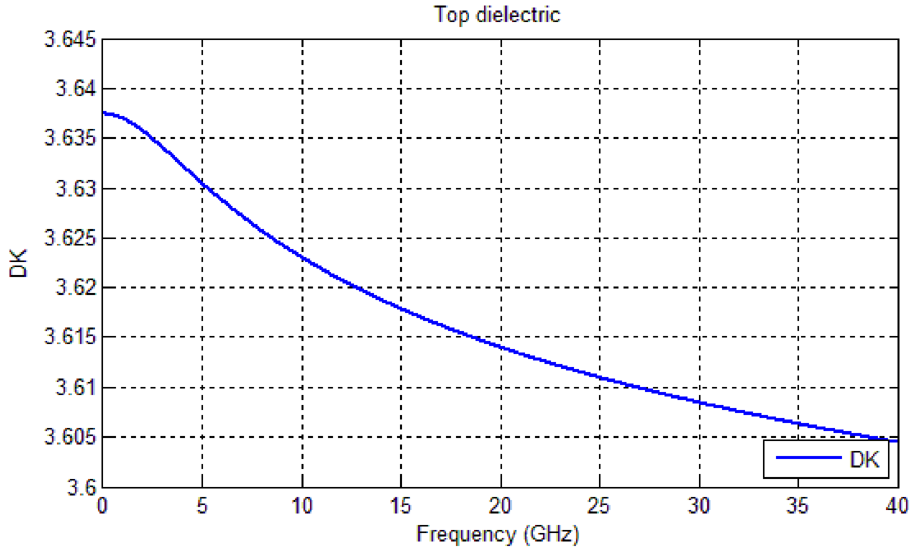


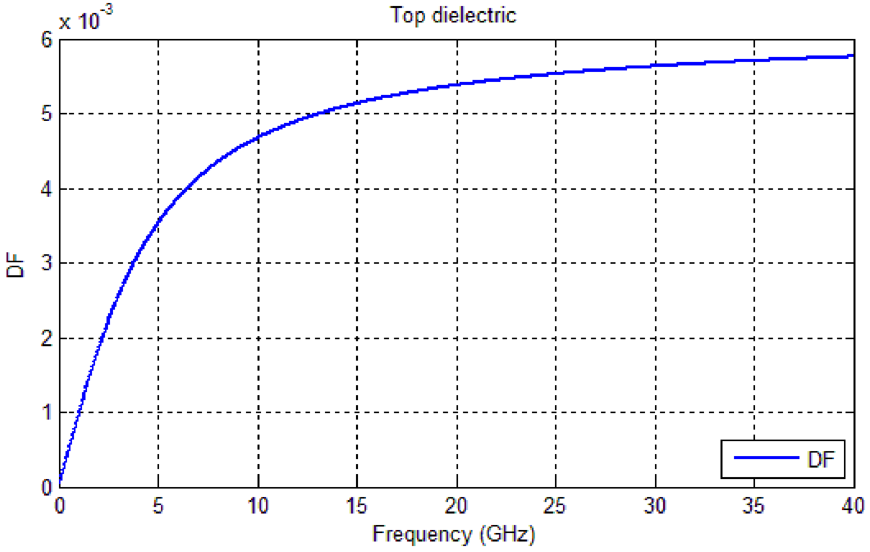
Extracted DK2, DF2



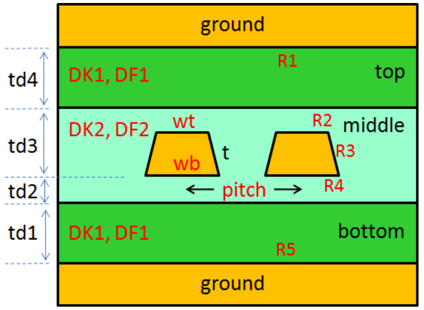
$$\varepsilon_\infty = 3.46724$$
$$\Delta\varepsilon = 0.170196$$
$$m1 = 9.58715$$
$$m2 = 14.8352$$

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$



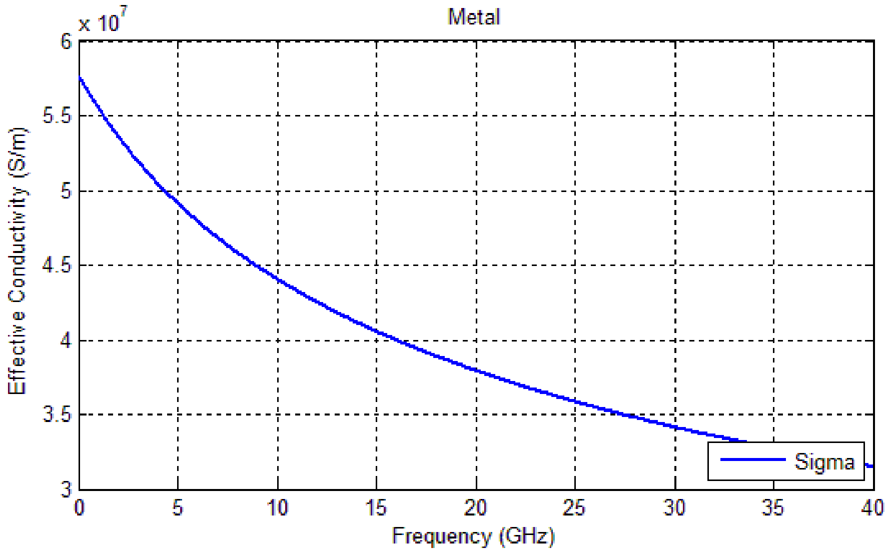


Extracted effective conductivity

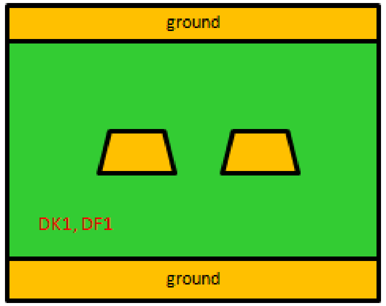


$$\sigma = 5.8 \times 10^{7}\ \text{S/m}$$

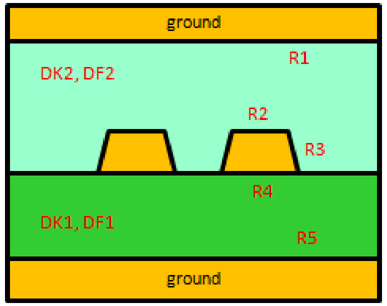
$$R_q = 0.324321\,\mu\text{m}$$



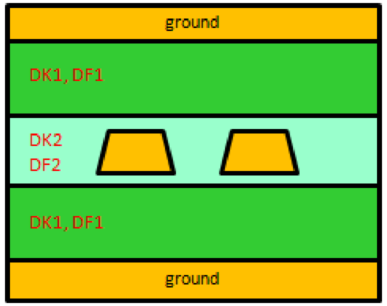
Comparison of Models 1 to 5



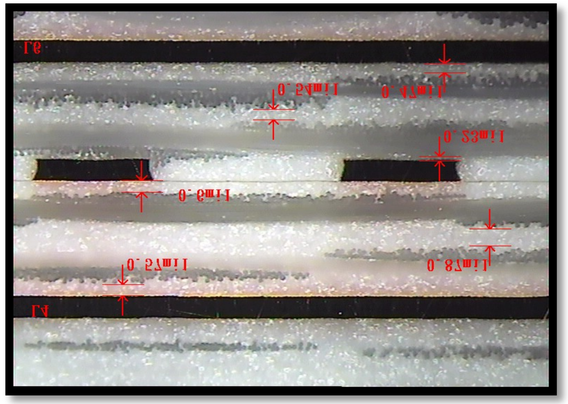
Model 1

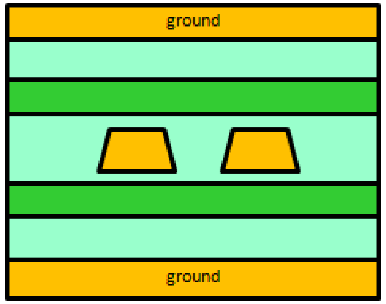


Model 2

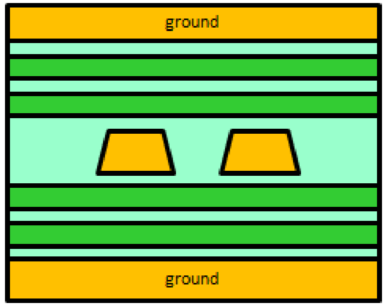


Model 3





Model 4



Model 5

Model	DK1	DK2
1	3.510	-
2	2.444	4.294
3	3.413	3.623
4	3.863	3.360
5	3.115	3.975

At 10 GHz

DK2>DK1 because of positive-polarity FEXT

References

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- Djordjevic, R.M. Biljic, V.D. Likar-Smiljanic, T.K.Sarkar, "Wideband Frequency-Domain Characterization of FR-4 and TimeDomain Causality," IEEE Trans. on EMC, vol. 43, No. 4, November 2001.
- J. Eric Bracken, "A causal Huray model for surface roughness," DesignCon 2012.
- Gerald Gold and Klaus Helmreich, "A physical surface roughness model and its applications," IEEE Tran. on Microwave Theory and Techniques, Vol. 65, No. 10, October 2017.
- Dusan N. Grujic, "Closed-form solution of rough conductor surface impedance," IEEE Trans. On Microwave Theory and Techniques, Vol. 66, No. 11, November 2018.
- C.C. Huang, "In-Situ De-embedding," EDI CON, Beijing, China, 04/19 to 04/21/2016.
- C. Luk, J. Buan, T. Ohshida, P.J. Wang, Y. Oryu, C.C. Huang and N. Jarvis, "Hacking skew measurement," DesignCon 2018, 01/30 to 02/01/2018, Santa Clara, CA.
- J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, "Aristotle: A fully automated SI platform for PCB material characterization," DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.

Outline

- Introduction : J. Balachandran - Cisco inc
- PCB Material Characterization Theory : Ching Chao Huang - Ataitec Corp
- Modeling PCB Interconnects : Alvin Wang - Hirose Electricals
- Addressing Skew impairments : Clement Luk, Samtec
- Test Fixture Design : Jeremy Baun - Hirose Electricals, J. Balachandran
- Automation : J. Balachandran
- Case Study & Results : Anna Gao – Cisco inc
- Summary : Ching Chao Huang

Modeling PCB Interconnets

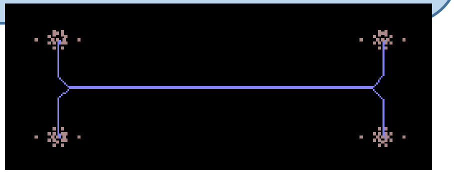
Outline

- PCB material property extraction flow
- Measured DUT vs. simulation
- Several ways to model DK, DF and roughness
  - Djordjevc-Sarkar model (for DK/DF)
  - Effective conductivity and Huray models (for roughness)
  - Tabular frequency-dependent DK, DF and conductivity
- Djordjevic-Sarkar model
  - Djordjevic vs. Svensson formats
- Huray model
  - Conversion from effective conductivity to Huray model
- How to specify tabular frequency-dependent DK, DF and conductivity in HFSS
- How to specify Djordjevic-Sarkar and Huray models in HFSS
- Measurement and extracted model for 2” stripline
  - Correlation between HFSS and X2D2* using various DK, DF and roughness models

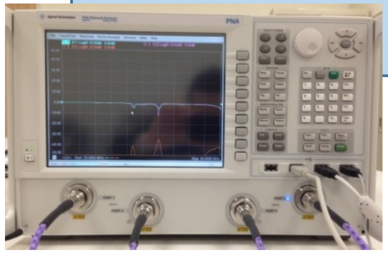
* X2D2 is a 2D solver from AtaiTec.

PCB material property extraction flow (1/2)

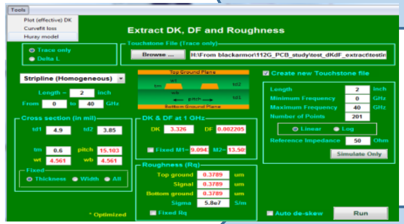
- PCB structure design
- Fixture-DUT-fixture
- Fixture-fixture (2X Thru)
- Single and differential trace design



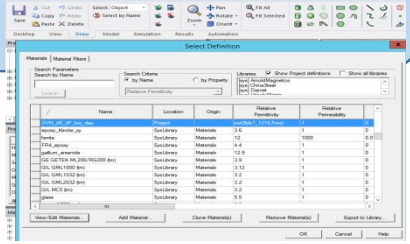
- VNA/probe measurement
- Different types of connector
- De-embedded



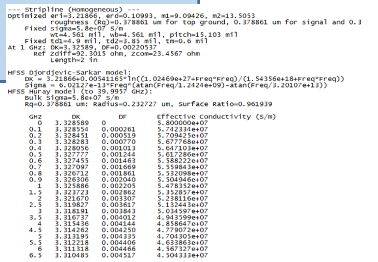
- Software tools (e.g., ADK) for material extraction
- Generated information needed for simulation (DK, DF, and conductivity……etc.)



- Implement DK, DF, and conductivity information into 2D or 3D solver



- Tabular frequency-dependent DK, DF, and conductivity
- Djordjevic-Sarkar model
- Huray model

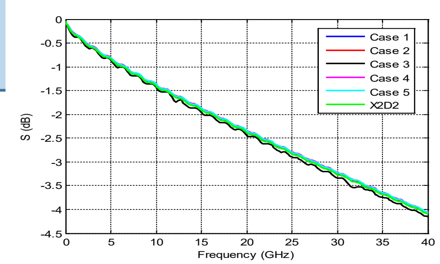


```
--- Stripline (Homogeneous) ---
Optimized eri=3.21866, erd=0.10993, m1=9.09426, m2=13.5053
          roughness (Rq)=0.378861 um for top ground, 0.378861 um for signal and 0.3
    Fixed sigma=5.8e+07 S/m
          wt=4.561 mil, wb=4.561 mil, pitch=15.103 mil
    Fixed td1=4.9 mil, td2=3.85 mil, tm=0.6 mil
At 1 GHz: DK=3.32589, DF=0.00220537
      Ref Zdiff=92.3015 ohm, Zcom=23.4567 ohm
          Length=2 in

HFSS Djordjevic-Sarkar model:
    DK = 3.21866+0.00541165*ln((1.02469e+27+Freq*Freq)/(1.54356e+18+Freq*Freq))
    Sigma = 6.02127e-13*Freq*(atan(Freq/1.2424e+09)-atan(Freq/3.20107e+13))
HFSS Huray model (to 39.9957 GHz):
    Bulk Sigma=5.8e+07 S/m
    Rq=0.378861 um: Radius=0.232727 um, Surface Ratio=0.961939
```

GHz	DK	DF	Effective Conductivity (S/m)
0	3.328589	0	5.800000e+07
0.1	3.328554	0.000261	5.742334e+07
0.2	3.328451	0.000519	5.709425e+07
0.3	3.328283	0.000770	5.677768e+07
0.4	3.328056	0.001013	5.647103e+07
0.5	3.327777	0.001244	5.617286e+07
0.6	3.327455	0.001463	5.588222e+07
0.7	3.327097	0.001669	5.559843e+07
0.8	3.326712	0.001861	5.532098e+07
0.9	3.326306	0.002040	5.504946e+07
1	3.325886	0.002205	5.478352e+07
1.5	3.323723	0.002862	5.352857e+07
2	3.321670	0.003307	5.238116e+07
2.5	3.319827	0.003617	5.132443e+07
3	3.318191	0.003843	5.034597e+07
3.5	3.316737	0.004012	4.943599e+07
4	3.315436	0.004144	4.858647e+07
4.5	3.314262	0.004250	4.779072e+07
5	3.313195	0.004335	4.704305e+07
5.5	3.312218	0.004406	4.633863e+07
6	3.311318	0.004466	4.567327e+07
6.5	3.310485	0.004517	4.504333e+07

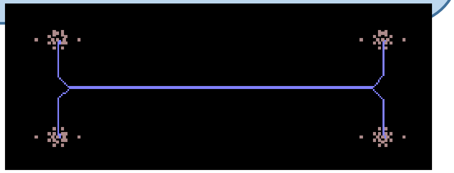
- Simulation setup
- Compared the simulation results



DESIGNCON 2019 WHERE THE CHIP MEETS THE BOARD

PCB material property extraction flow (2/2)

- PCB structure design
- Fixture-DUT-fixture
- Fixture-fixture (2X Thru)
- Single and differential trace design



- VNA/probe measurement
- Different types of connector
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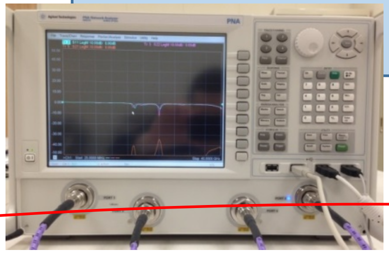

- Software tools (e.g. ADK) for material extraction
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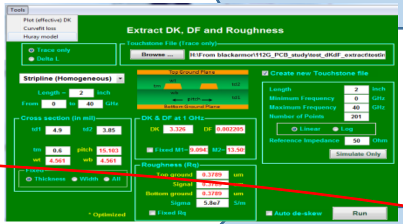
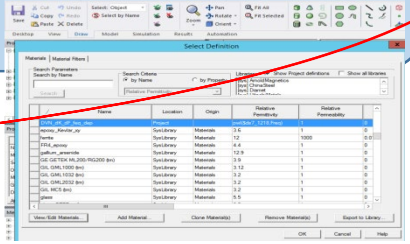
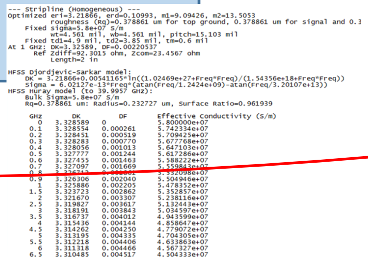


- Implement DK, DF, and conductivity information into 2D or 3D solver



- Tabular frequency-dependent DK, DF, and conductivity
- Djordjevic-Sarkar model
- Huray model



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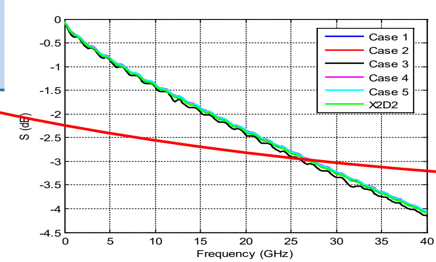
    Sigma = 6.02127e-13*Freq*(atan(Freq/1.2424e+09)-atan(Freq/3.20107e+13))
HFSS Huray model (to 39.9957 GHz):
    Bulk Sigma=5.8e+07 S/m
    Rq=0.378861 um: Radius=0.232727 um, Surface Ratio=0.961939

     GHz       DK         DF         Effective Conductivity (S/m)
       0    3.328589   0            5.800000e+07
     0.1    3.328554   0.000261     5.742334e+07
     0.2    3.328451   0.000519     5.709425e+07
     0.3    3.328283   0.000770     5.677768e+07
     0.4    3.328056   0.001013     5.647103e+07
     0.5    3.327777   0.001244     5.617286e+07
     0.6    3.327455   0.001463     5.588222e+07
     0.7    3.327097   0.001669     5.559843e+07
     0.8    [illegible] [illegible]  5.532098e+07
     0.9    3.326306   0.002040     5.504946e+07
       1    3.325886   0.002205     5.478352e+07
     1.5    3.323723   0.002862     5.352857e+07
       2    3.321670   0.003307     5.238116e+07
     2.5    3.319827   0.003617     5.132443e+07
       3    3.318191   0.003843     5.034597e+07
     3.5    3.316737   0.004012     4.943599e+07
       4    3.315436   0.004144     4.858647e+07
     4.5    3.314262   0.004250     4.779072e+07
       5    3.313195   0.004335     4.704305e+07
     5.5    3.312218   0.004406     4.633863e+07
       6    3.311318   0.004466     4.567327e+07
     6.5    3.310485   0.004517     4.504333e+07
```

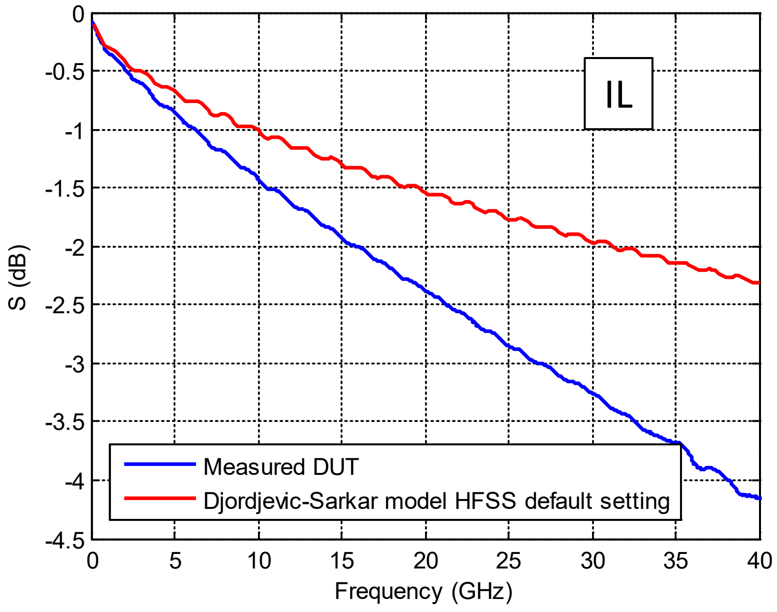
- Simulation setup
- Compared the simulation results



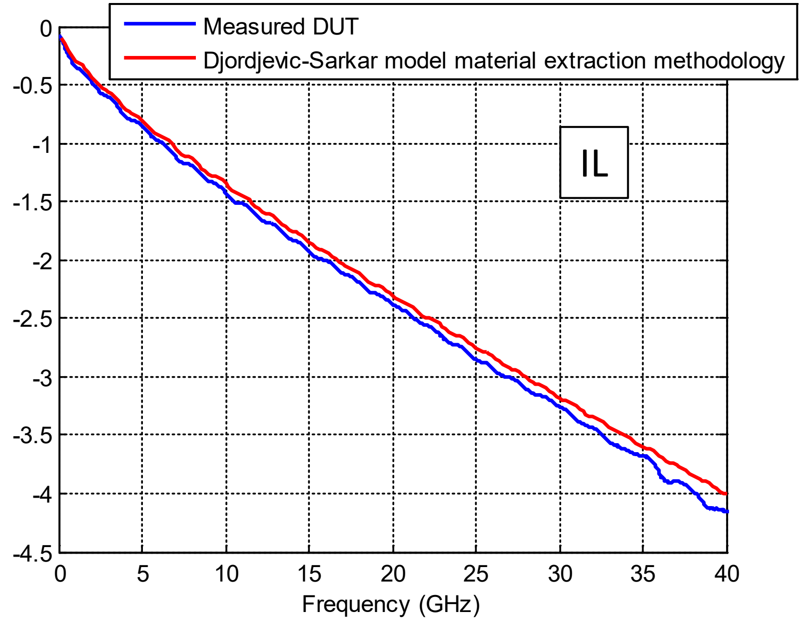
Modeling session covers these topics!!

De-embedded DUT (measured) vs. HFSS simulation with DK & DF @1GHz

- DK and DF values are usually given at 1GHz.
- Djordjevic-Sarkar model default setting => poor correlation.
- Djordjevic-Sarkar model PCB material extraction => good correlation.



Default



D-S model from MPX extraction methodology

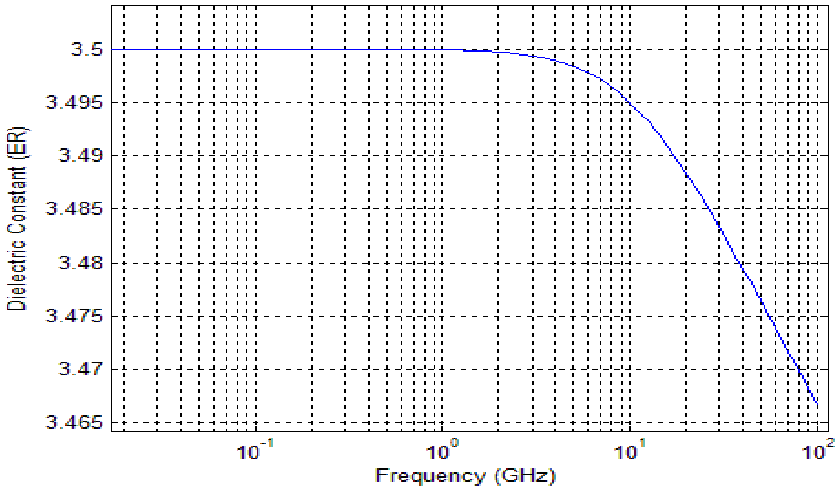
WHY??

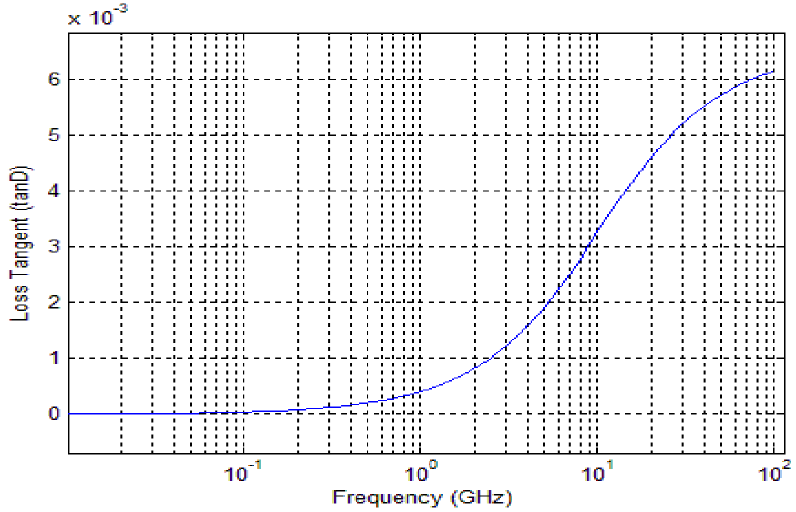
- We need PCB material property extraction to higher frequencies
- Implement frequency-dependent DK, DF, and conductivity
- Implement Huray model
- Implement Djordjevic-Sarkar model

Djordjevic-Sarkar model (for DK/DF)

- Need only four variables: ε_∞ , $\Delta\varepsilon$, m_1 , m_2 to represent wide-band DK & DF.

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$





$\varepsilon_\infty = 3.35$, $\Delta\varepsilon = 0.15$, $m_1 = 10$, $m_2 = 14.5$

Djordjevic and Svensson formats are equivalent.

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$

$$= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{f_2 + i \cdot f}{f_1 + i \cdot f}\right)$$

$$= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{A \cdot e^{i\phi_2}}{B \cdot e^{i\phi_1}}\right)$$

$$= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \log_e\left(\frac{A \cdot e^{i\phi_2}}{B \cdot e^{i\phi_1}}\right)$$

$$= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \left\{\log_e\left(\frac{A}{B}\right) + i(\phi_2 - \phi_1)\right\}$$

$$= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \left\{\frac{1}{2}\log_e\left(\frac{f_2^2 + f^2}{f_1^2 + f^2}\right) + i\left(\tan^{-1}\left(\frac{f}{f_2}\right) - \tan^{-1}\left(\frac{f}{f_1}\right)\right)\right\}$$

$$= \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \frac{1}{\log_e(10)} \cdot \left\{\frac{1}{2}\log_e\left(\frac{\tau_2^2\left(1 + \omega^2\tau_1^2\right)}{\tau_1^2\left(1 + \omega^2\tau_2^2\right)}\right) + i\left(\tan^{-1}(\omega\tau_1) - \tan^{-1}(\omega\tau_2)\right)\right\}$$

$$= \varepsilon_r \cdot (1 - i\tan\delta)$$

$$= \varepsilon_r \cdot \left(1 - i\frac{\sigma}{2\pi f \varepsilon_r \varepsilon_0}\right)$$

X2D2* ← $\varepsilon_\infty \quad \Delta\varepsilon \quad m_1 \quad m_2$

* X2D2 is a 2D solver from AtaiTec (www.ataitec.com)

Djordjevic format

Svensson format

HFSS →

$$\begin{cases} \varepsilon_r = \varepsilon_\infty + \Delta\varepsilon \cdot \dfrac{1}{m_2 - m_1} \cdot \dfrac{1}{\log_e(10)} \cdot \dfrac{1}{2}\log_e\left(\dfrac{f_2^2 + f^2}{f_1^2 + f^2}\right) \\ \sigma = 2\pi f \cdot \varepsilon_0 \cdot \Delta\varepsilon \cdot \dfrac{1}{m_2 - m_1} \cdot \dfrac{1}{\log_e(10)} \cdot \left(\tan^{-1}\left(\dfrac{f}{f_1}\right) - \tan^{-1}\left(\dfrac{f}{f_2}\right)\right) \end{cases}$$

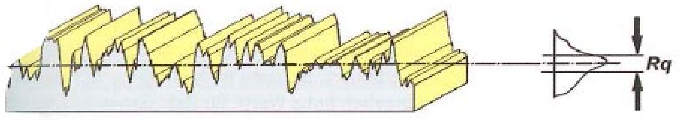
Effective conductivity model (for surface roughness)

- Effective conductivity* (by G. Gold & K. Helmreich at DesignCon 2014) needs only two variables: σ_{bulk} , R_q

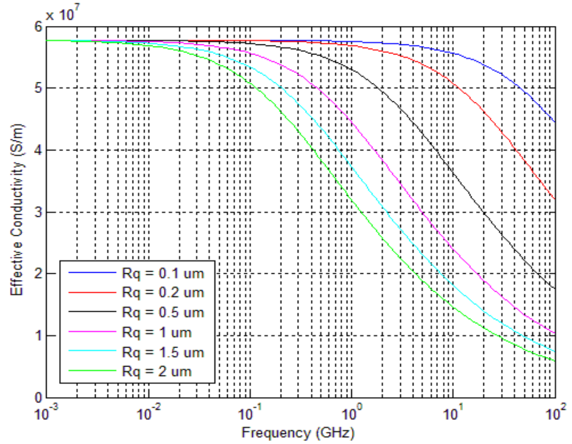
Parameter	Description	Standard
R_q	root mean square	DIN EN ISO 4287
R_a	arithmetic average	DIN EN ISO 4287, ANSI B 46.1
R_k	core roughness depth	DIN EN ISO 13565
R_z	average surface roughness	DIN EN ISO 4287

Table 1: *Statistical parameters to describe surface roughness*

$$\sigma(x) = \sigma_{bulk} \cdot CDF(x) = \sigma_{bulk} \cdot \int_{-\infty}^{x} PDF(x) du = \sigma_{bulk} \cdot \int_{-\infty}^{x} e^{-\frac{u^2}{2R_q^2}} du$$



- Numerically solving $\nabla^2 \overline{B} - j\omega\mu\sigma\overline{B} + \frac{\nabla\sigma}{\sigma} \times (\nabla \times \overline{B}) = 0$ and equating power to that of smooth surface gives σ_{eff}
- A recent paper (by D.N. Grujic in MTT, Nov. 2018) gives closed-form equation.



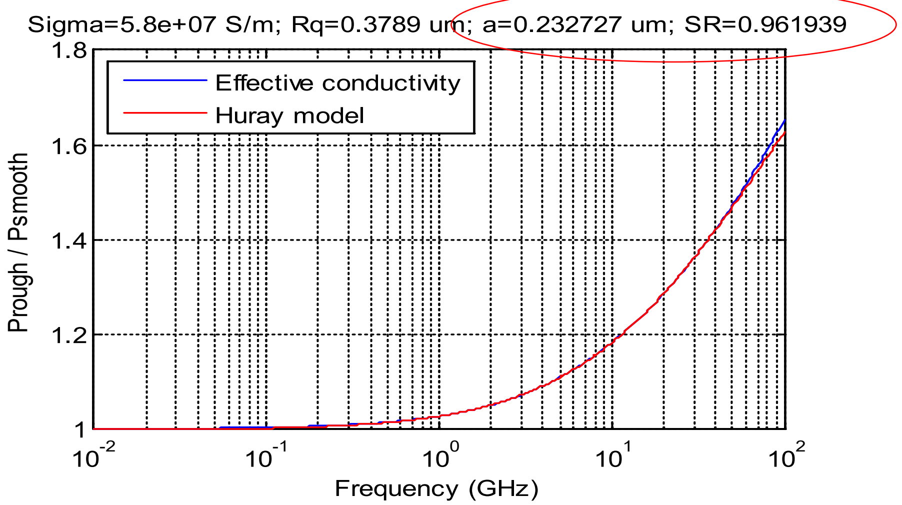
Convert effective conductivity to Huray model

- Huray model

$$\frac{P_{rough}}{P_{smooth}} \approx 1 + \frac{3}{2} \cdot SR \cdot \left(\frac{1}{1 + \frac{\delta(f)}{a} + \frac{1}{2}\left(\frac{\delta(f)}{a}\right)^2} \right)$$

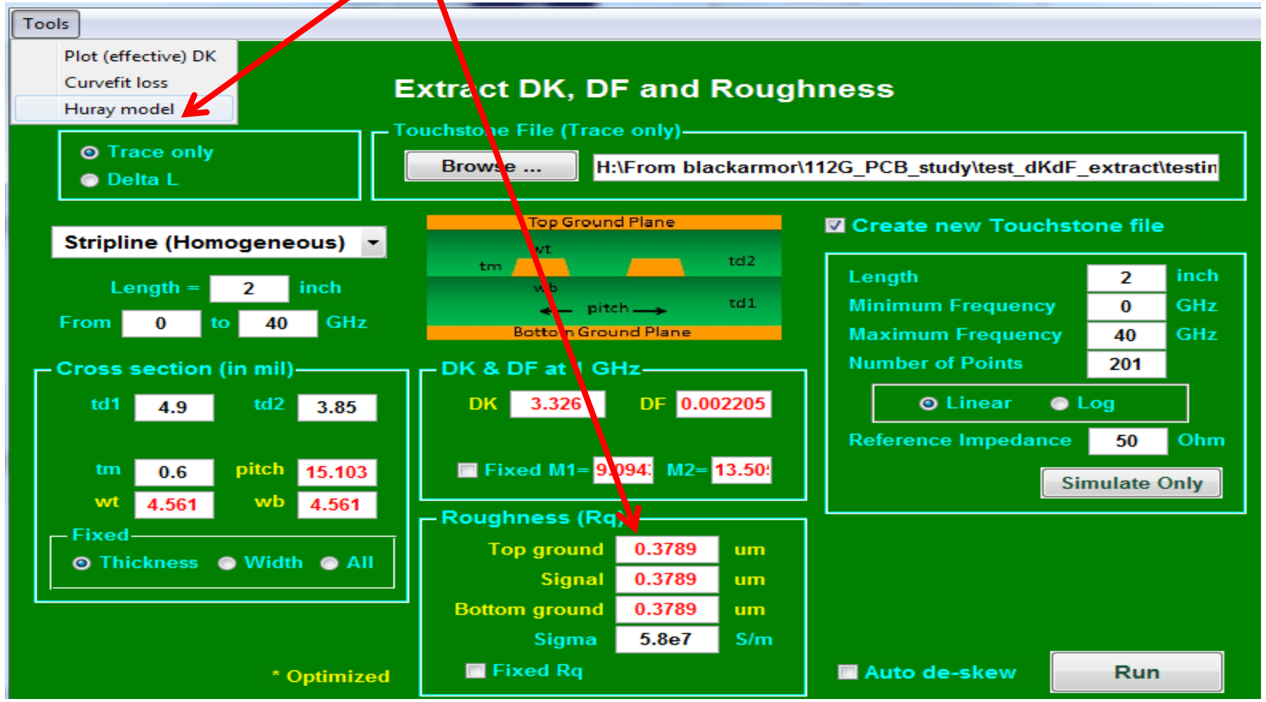
$$\delta(f) = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad ; \quad a = \text{radius} \quad ; \quad SR = \text{surface ratio}$$

- Curvefit Prough / Psmooth to convert σ_{bulk} , R_q (in X2D2) to a , SR (in HFSS)

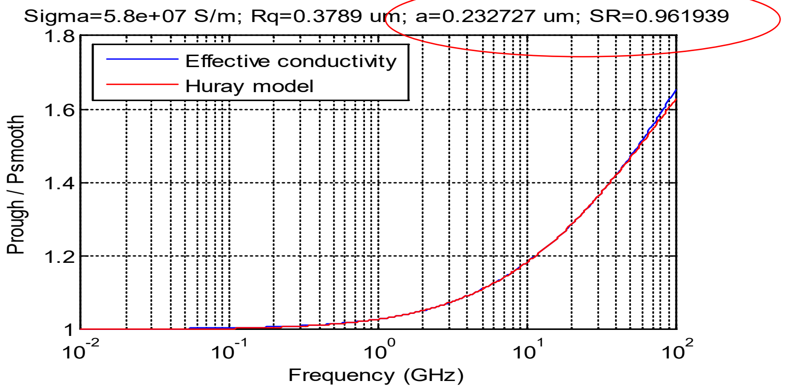


Automated conversion* from effective conductivity to Huray model

Input bulk conductivity and roughness
and click Huray model



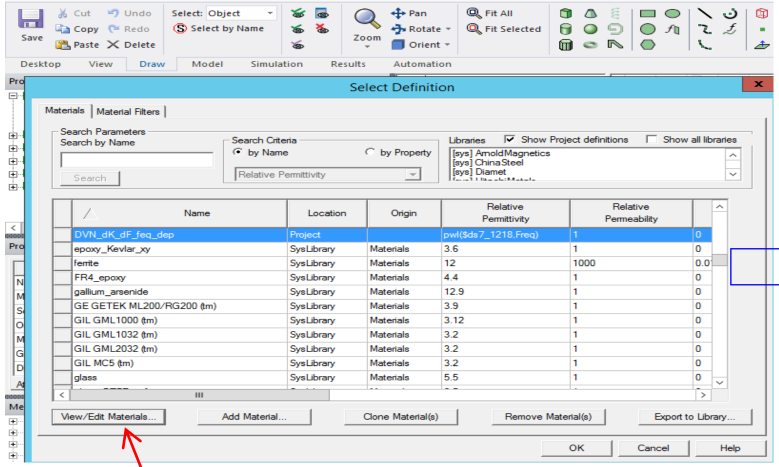
Needed for HFSS

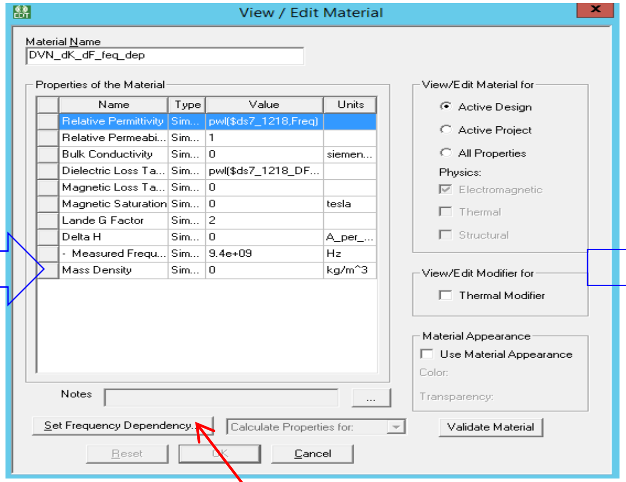


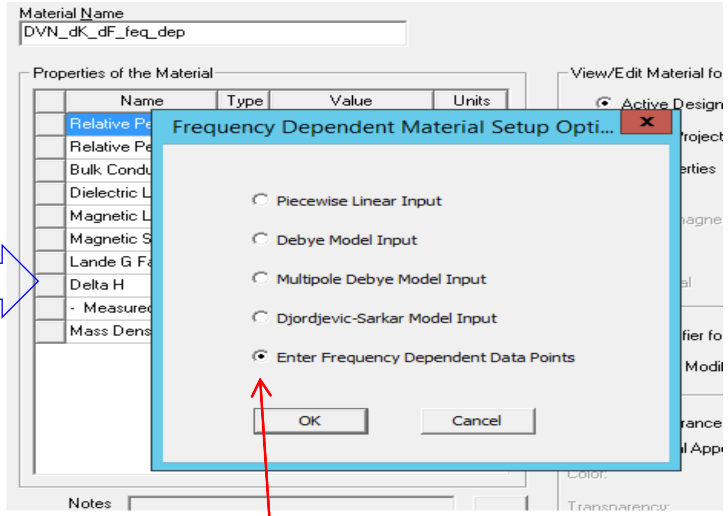
* ADK from AtaiTec.

HFSS setup

How to specify tabular frequency-dependent DK, DF and conductivity (1/2)







Select "View/Edit Materials"

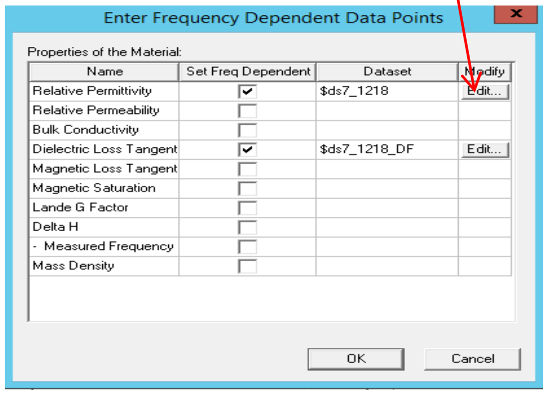
Select "Set Frequency Dependency"

Select "Enter Frequency Dependent Data Points"

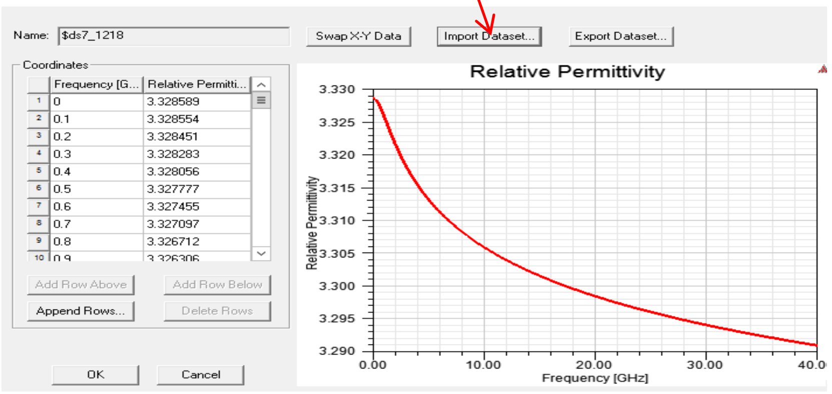
HFSS setup

How to specify tabular frequency-dependent DK, DF and conductivity (2/2)

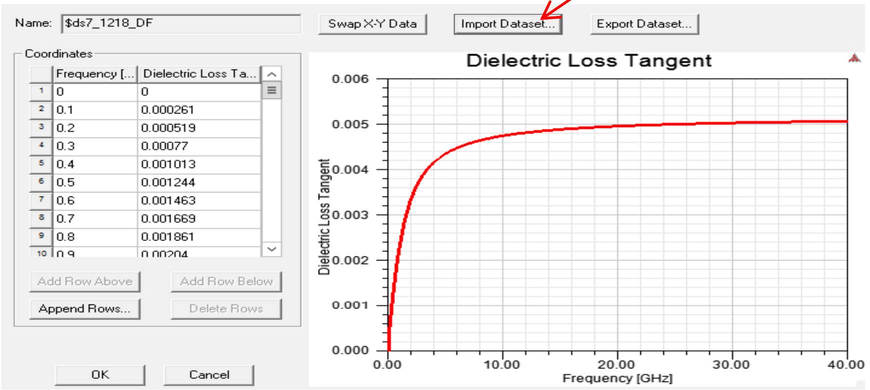
Select "Edit"



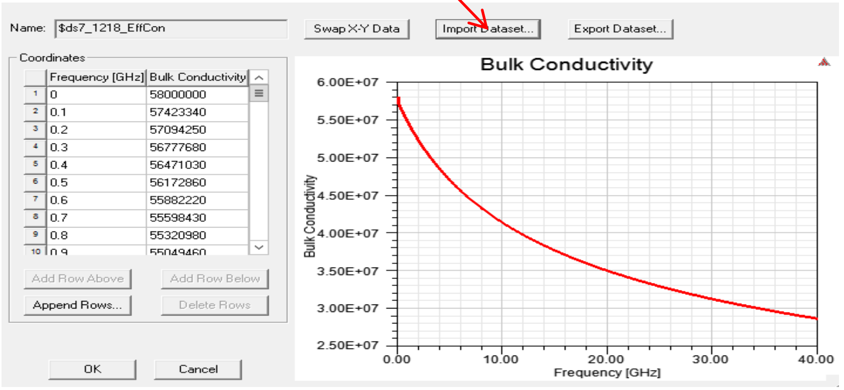
Import dataset* for permittivity



Import dataset* for DF



Import dataset* for conductivity




```
--- Stripline (Homogeneous) ---
Optimized eri=3.21866, erd=0.10993, m1=9.09426, m2=13.5053
          roughness (Rq)=0.378861 um for top ground, 0.378861 um for signal and 0.3
    Fixed sigma=5.8e+07 S/m
          wt=4.561 mil, wb=4.561 mil, pitch=15.103 mil
    Fixed td1=4.9 mil, td2=3.85 mil, tm=0.6 mil
At 1 GHz: DK=3.32589, DF=0.00220537
      Ref Zdiff=92.3015 ohm, Zcom=23.4567 ohm
          Length=2 in

HFSS Djordjevic-Sarkar model:
    DK = 3.21866+0.00541165*ln((1.02469e+27+Freq*Freq)/(1.54356e+18+Freq*Freq))
    Sigma = 6.02127e-13*Freq*(atan(Freq/1.2424e+09)-atan(Freq/3.20107e+13))
HFSS Huray model (to 39.9957 GHz):
    Bulk Sigma=5.8e+07 S/m
    Rq=0.378861 um: Radius=0.232727 um, Surface Ratio=0.961939
```

GHz	DK	DF	Effective Conductivity (S/m)
0	3.328589	0	5.800000e+07
0.1	3.328554	0.000261	5.742334e+07
0.2	3.328451	0.000519	5.709425e+07
0.3	3.328283	0.000770	5.677768e+07
0.4	3.328056	0.001013	5.647103e+07
0.5	3.327777	0.001244	5.617286e+07
0.6	3.327455	0.001463	5.588222e+07
0.7	3.327097	0.001669	5.559843e+07
0.8	3.326712	0.001861	5.532098e+07
0.9	3.326306	0.002040	5.504946e+07
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2	3.321670	0.003307	5.238116e+07
2.5	3.319827	0.003617	5.132443e+07
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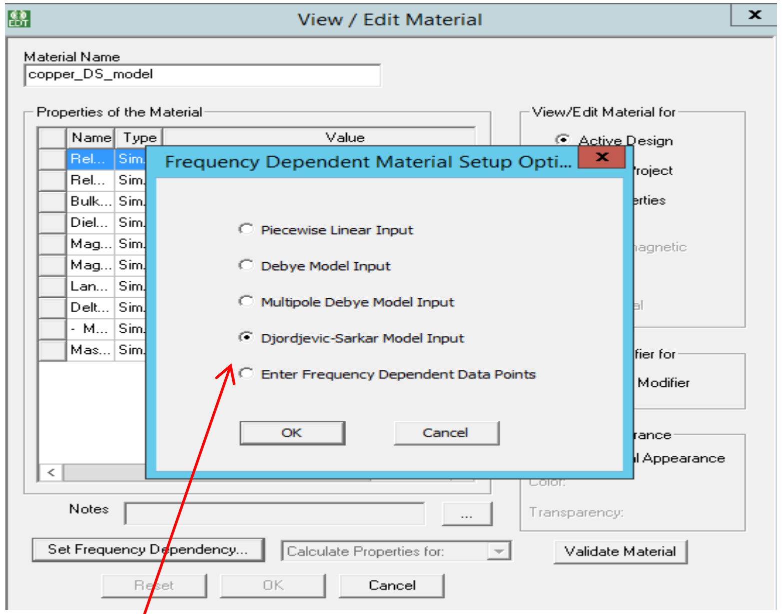
4	3.315436	0.004144	4.858647e+07
4.5	3.314262	0.004250	4.779072e+07
5	3.313195	0.004335	4.704305e+07
5.5	3.312218	0.004406	4.633863e+07
6	3.311318	0.004466	4.567327e+07
6.5	3.310485	0.004517	4.504333e+07

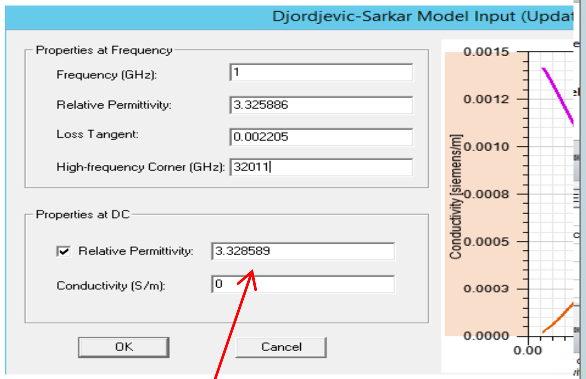
* Frequency-dependent table from ADK

HFSS setup

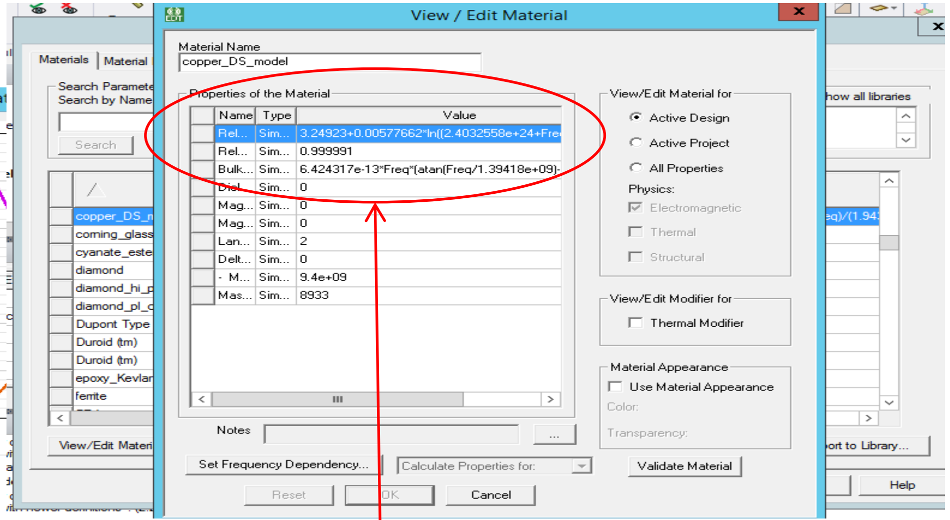
How to specify Djordjevic-Sarkar model



Select Djordjevic-Sarkar model



Enter parameters



Copy/paste equations from ADK output if necessary.

```
HFSS Djordjevic-Sarkar model:
    DK = 3.21866+0.00541165*ln((1.02469e+27+Freq*Freq)/(1.54356e+18+Freq*Freq))
    Sigma = 6.02127e-13*Freq*(atan(Freq/1.2424e+09)-atan(Freq/3.20107e+13))
HFSS Huray model (to 39.9957 GHz):
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0.3	3.328283	0.000770	5.677768e+07
0.4	3.328056	0.001013	5.647103e+07
0.5	3.327777	0.001244	5.617286e+07
0.6	3.327455	0.001463	5.588222e+07

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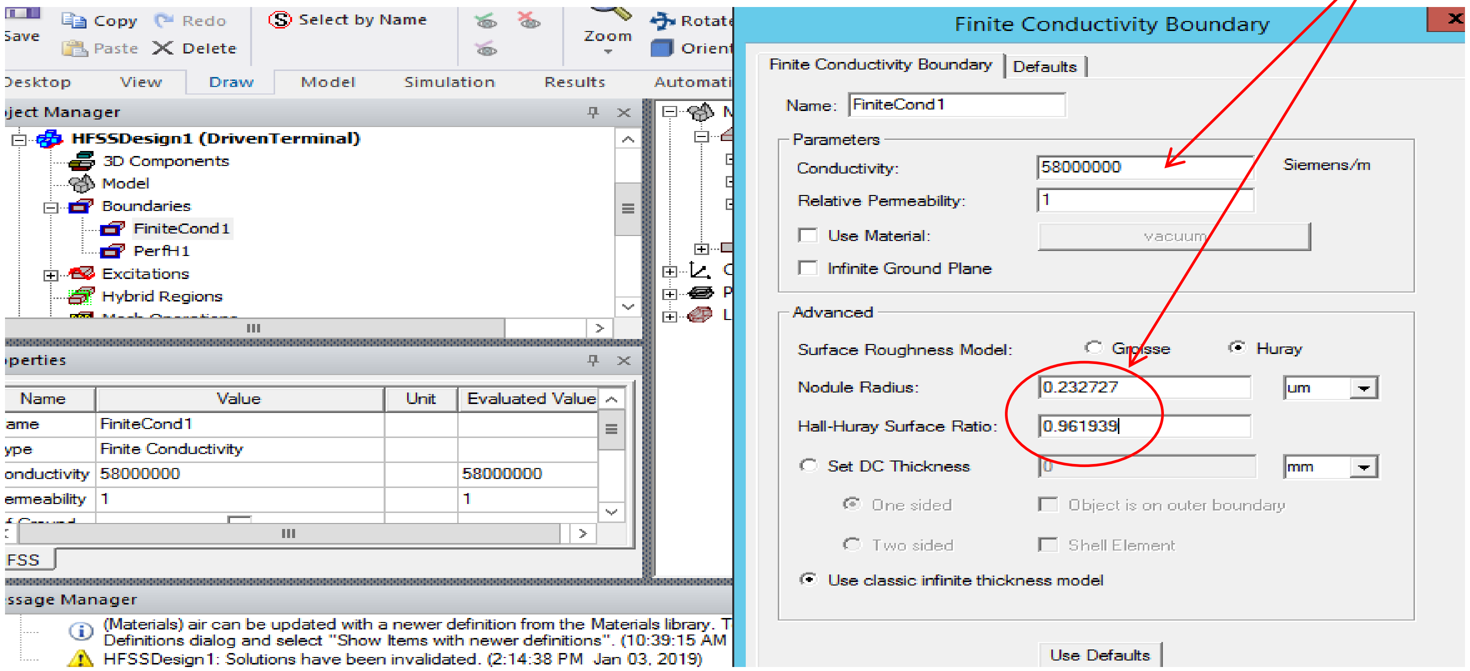
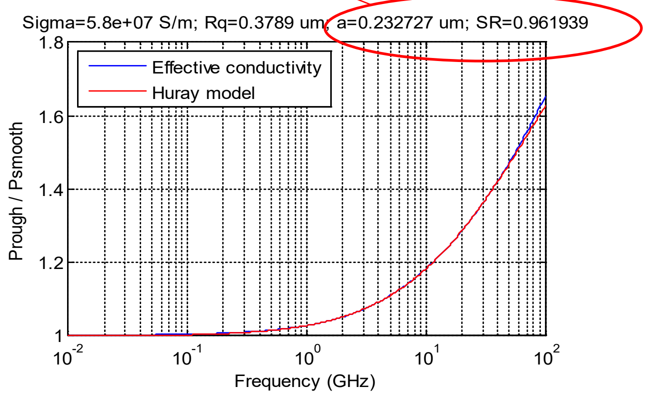
HFSS setup
How to specify Huray model

Enter parameters from ADK output






```
HFSS Djordjevic-Sarkar model:
    DK = 3.21866+0.00541165*ln((1.02469e+27+Freq*Freq)/(1.54356e+18+Freq*Freq))
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HFSS Huray model (to 39.9957 GHz):
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     GHz      DK          DF         Effective Conductivity (S/m)
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     0.3    3.328283    0.000770     5.677768e+07
     0.4    3.328056    0.001013     5.647103e+07
     0.5    3.327777    0.001244     5.617286e+07
     0.6    3.327455    0.001463     5.588222e+07
```
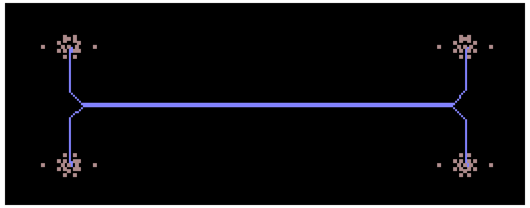
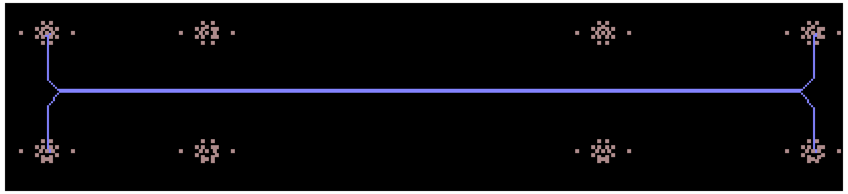

Measurement

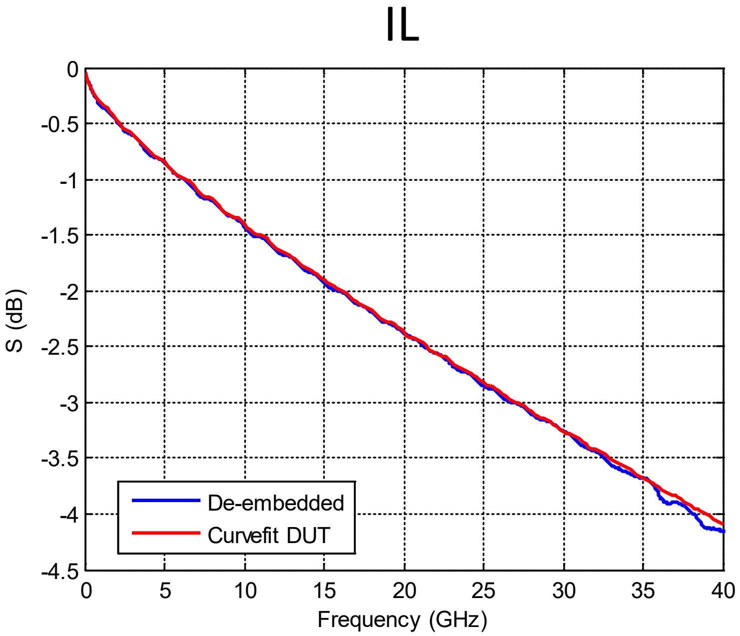
- De-embed 2” trace from 4” trace and curvefit DUT (the remaining 2” trace) with homogeneous stripline model*.

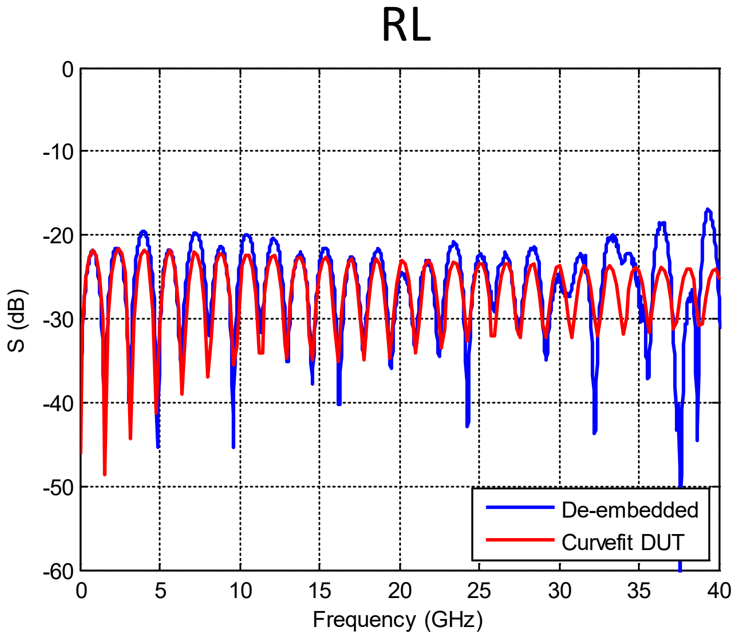
2 inch trace



4 inch trace



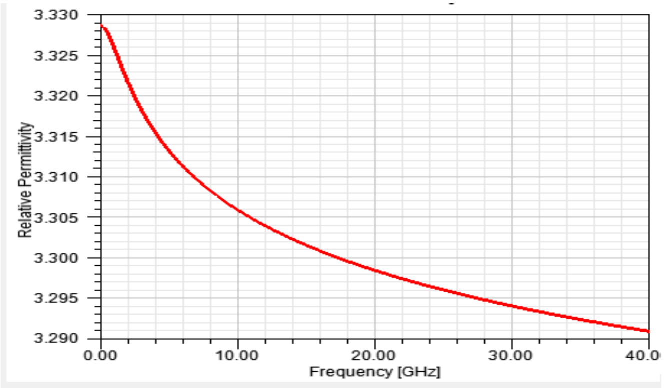




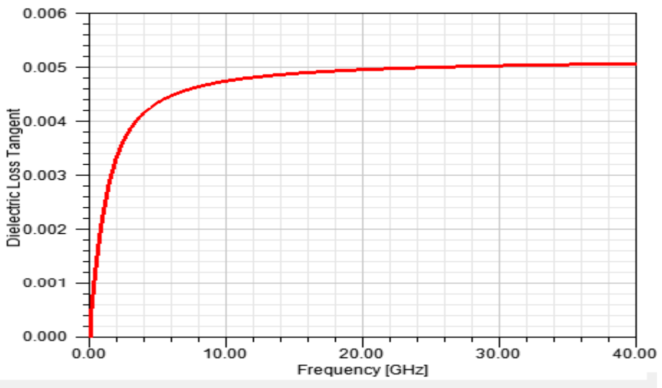
* Using ISD, ADK and X2D2 from AtaiTec.

Extracted frequency-dependent DK, DF & conductivity

DK



DF



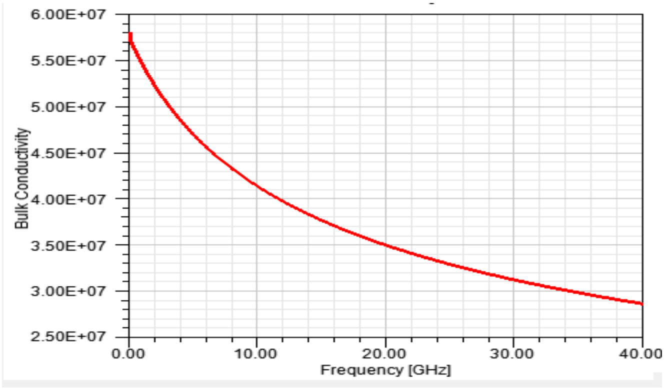
$$\varepsilon_\infty = 3.21866$$

$$\Delta\varepsilon = 0.10993$$

$$m_1 = 9.09426$$

$$m_2 = 13.5053$$

Effective Conductivity



$$\sigma_{bulk} = 5.8\times 10^7 \text{ S/m}$$

$$R_q = 0.378861\ \mu\text{m}$$

HFSS comparison
Create models from extracted results

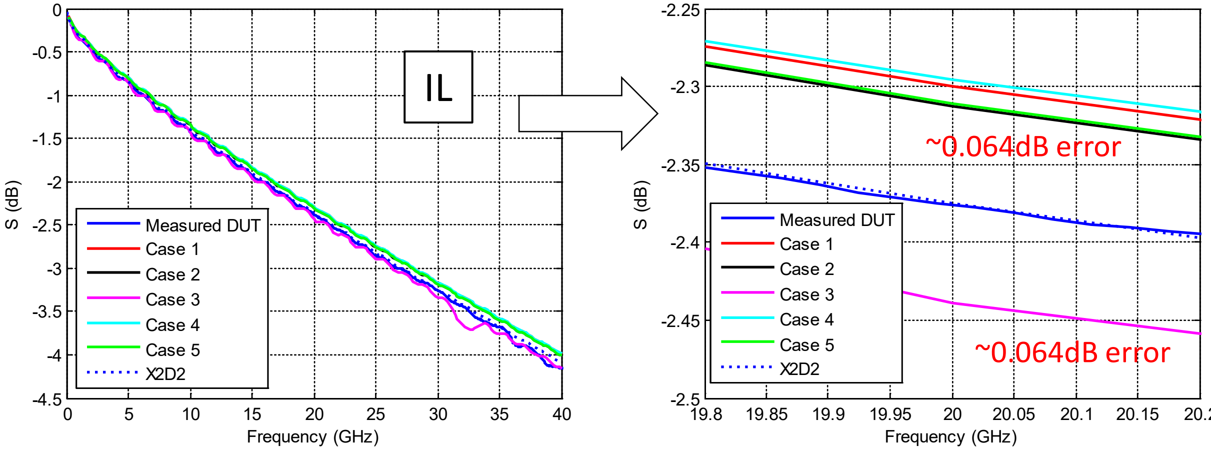
2” stripline
(Cascaded by 20 x 0.1” trace)

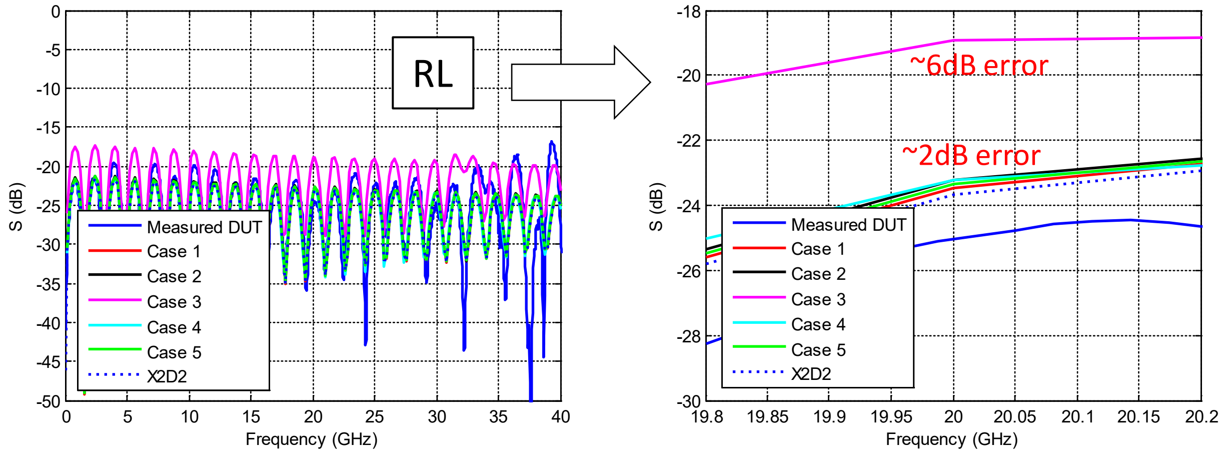
Case	Solver	DK/DF model	Roughness model	Delta S	Note
1	HFSS	Tabular DK/DF	Tabular conductivity	0.00008	Convergence test
2	HFSS	Tabular DK/DF	Tabular conductivity	0.0003	"
3	HFSS	Tabular DK/DF	Tabular conductivity	0.001	"
4	HFSS	Tabular DK/DF	Huray model	0.00008	Equivalent Huray model
5	HFSS	Djordjevic-Sarkar	Tabular conductivity	0.00008	Explicit equation in Svensson format
6	X2D2	Djordjevic-Sarkar	Effective conductivity	n/a	4 variables for Djordjevic format; 2 variables for effective conductivity

Differential IL & RL

- Compared various simulations with de-embedded DUT (measurement).
- Measured DUT, HFSS (except Case 3) and 2D solver (X2D2) correlate very well.
    - Case 3 was simulated with larger delta S.

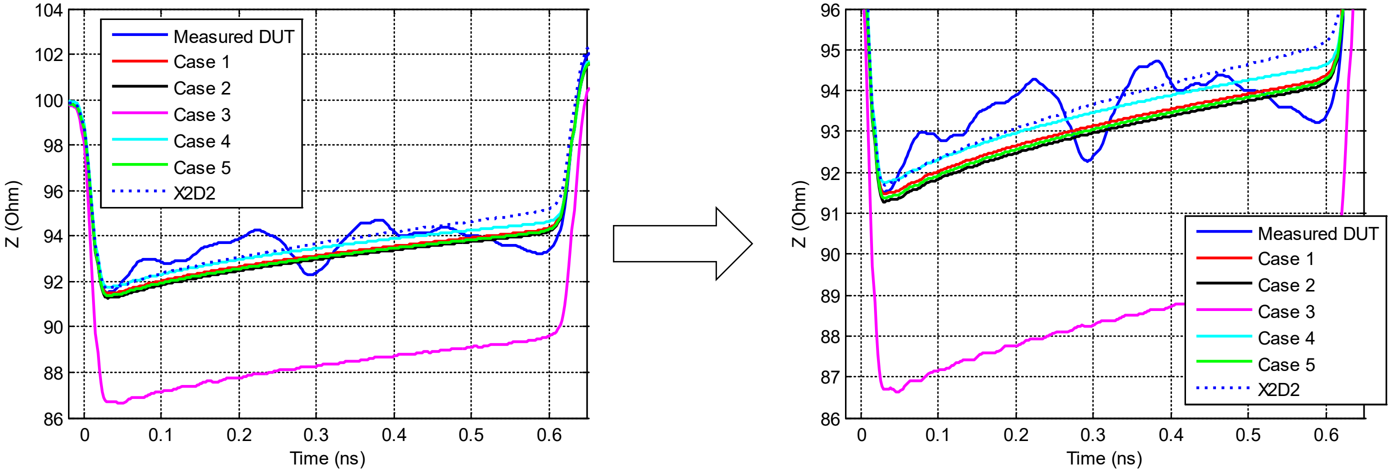
Case	Solver	DK/DF model	Roughness model	Delta S
1	HFSS	Tabular DK/DF	Tabular conductivity	0.00008
2	HFSS	Tabular DK/DF	Tabular conductivity	0.0003
3	HFSS	Tabular DK/DF	Tabular conductivity	0.001
4	HFSS	Tabular DK/DF	Huray model	0.00008
5	HFSS	Djordjevic-Sarkar	Tabular conductivity	0.00008
6	X2D2	Djordjevic-Sarkar	Effective conductivity	n/a





Differential TDR @ 12.5ps rise time

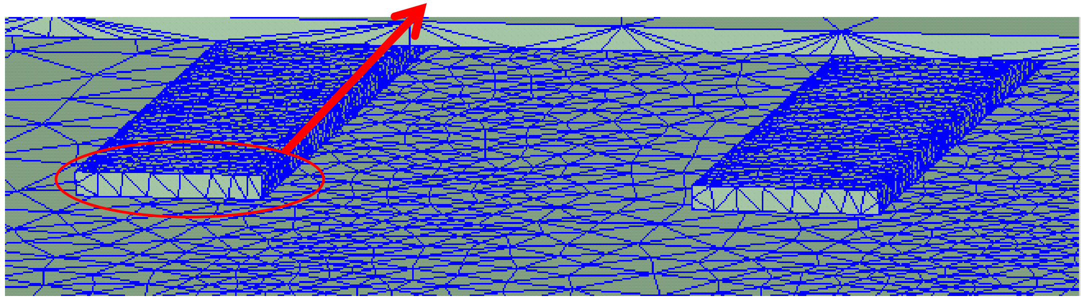
- Compared various simulations with de-embedded DUT (measurement).
- Measured DUT, HFSS (except Case 3) and 2D solver (X2D2) correlate very well.
  - Case 3 was simulated with larger delta S.



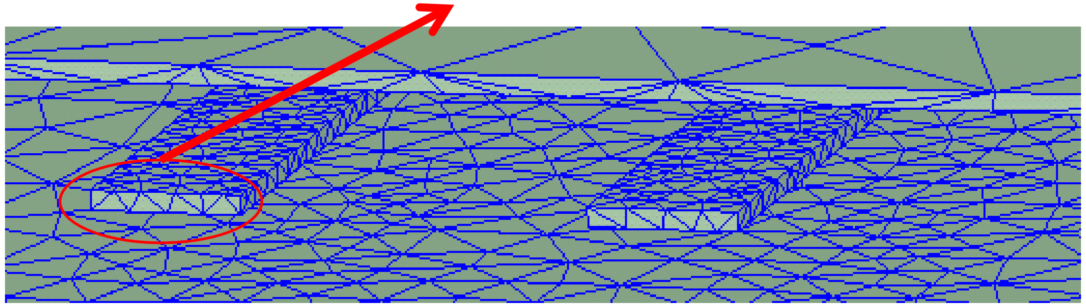
Case	Solver	DK/DF model	Roughness model	Delta S
1	HFSS	Tabular DK/DF	Tabular conductivity	0.00008
2	HFSS	Tabular DK/DF	Tabular conductivity	0.0003
3	HFSS	Tabular DK/DF	Tabular conductivity	0.001
4	HFSS	Tabular DK/DF	Huray model	0.00008
5	HFSS	Djordjevic-Sarkar	Tabular conductivity	0.00008
6	X2D2	Djordjevic-Sarkar	Effective conductivity	n/a

HFSS and X2D2 meshes

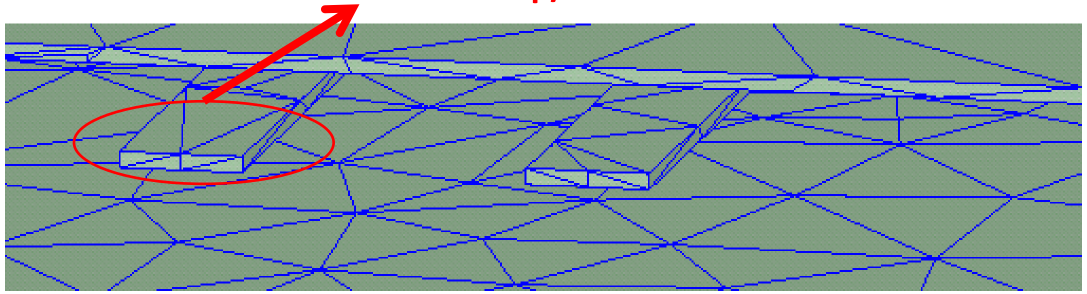
Case 1 7-8 meshes at top/bottom



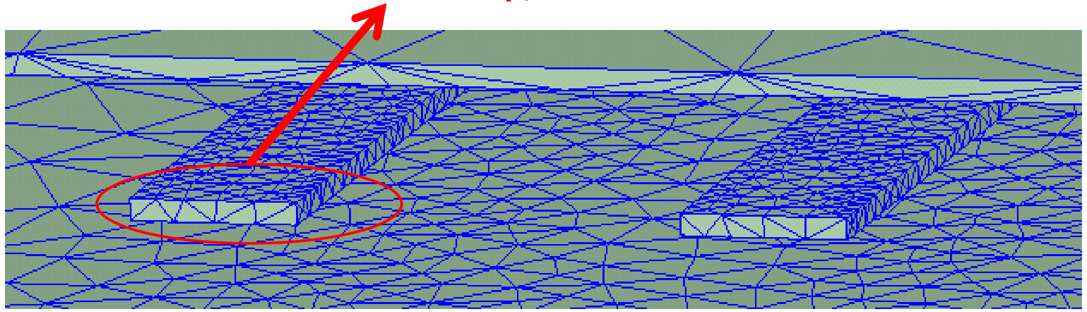
Case 2 4-6 meshes at top/bottom



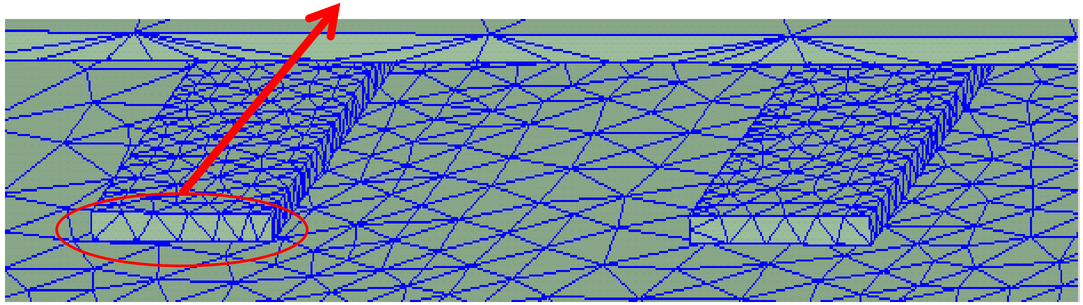
Case 3 2 meshes at top/bottom



Case 4 4-5 meshes at top/bottom

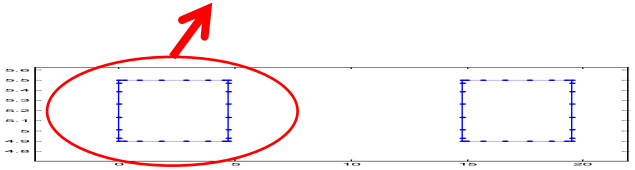


Case 5 5-6 meshes at top/bottom



Case 6

7 meshes on all sides



Number of meshes vs. convergence

Case 1 used ~ 634K meshes

Number of Passes: Completed 49, Maximum 55, Minimum 1
Max Mag. Delta S: Target 8E-05, Current 7.6311e-05
View: Table / Plot
Export...
CONVERGED
Consecutive Passes: Target 1, Current 1
Default Settings: Save Defaults, Clear Defaults

Pass Number	Solved Elements	Max Mag. Delta S
34	19851	0.0015892
35	23773	0.00094979
36	30125	0.0010584
37	37326	0.00075606
38	47402	0.00069452
39	60340	0.0004646
40	76873	0.00038453
41	90656	0.0002484
42	115599	0.00027075
43	147434	0.00022189
44	188466	0.0001858
45	241067	0.00015711
46	308691	0.00014061
47	395520	0.00012114
48	494095	9.0065e-05
49	634254	7.6311e-05

Case 2 used ~ 112K meshes

Number of Passes: Completed 41, Maximum 55, Minimum 1
Max Mag. Delta S: Target 0.0003, Current 0.00022506
View: Table / Plot
Export...
CONVERGED
Consecutive Passes: Target 1, Current 1
Default Settings: Save Defaults, Clear Defaults

Pass Number	Solved Elements	Max Mag. Delta S
26	5857	0.00049944
27	6111	0.00051401
28	6380	0.00035856
29	8101	0.0033456
30	10304	0.0025679
31	13161	0.0018581
32	16762	0.0017191
33	20113	0.0010384
34	24463	0.00090358
35	30855	0.00095637
36	36838	0.00070047
37	46793	0.0006122
38	57926	0.0004151
39	73734	0.00039379
40	93932	0.00033261
41	112323	0.00022506

Case 3 used ~ 3K meshes

Number of Passes: Completed 17, Maximum 55, Minimum 1
Max Mag. Delta S: Target 0.001, Current 0.0005102
View: Table / Plot
Export...
CONVERGED
Consecutive Passes: Target 1, Current 1
Default Settings: Save Defaults, Clear Defaults

Pass Number	Solved Elements	Max Mag. Delta S
2	1622	0.18633
3	1625	0.0071873
4	1739	0.0093397
5	1863	0.011165
6	1989	0.010865
7	2134	0.0083652
8	2278	0.0020608
9	2408	0.005395
10	2564	0.0049346
11	2714	0.012987
12	2883	0.0030462
13	3056	0.0027188
14	3216	0.002959
15	3397	0.0015831
16	3584	0.0023377
17	3735	0.0005102

Case 4 used ~ 150K meshes

Number of Passes: Completed 44, Maximum 55, Minimum 1
Max Mag. Delta S: Target 8E-05, Current 7.6441e-05
View: Table / Plot
Export...
CONVERGED
Consecutive Passes: Target 1, Current 1
Default Settings: Save Defaults, Clear Defaults

Pass Number	Solved Elements	Max Mag. Delta S
29	9592	0.0028818
30	12227	0.0024362
31	15596	0.0014726
32	18850	0.0013198
33	23546	0.0011776
34	27405	0.00069273
35	34745	0.00092133
36	44077	0.0007221
37	56012	0.00051923
38	67385	0.00032148
39	75292	0.00018269
40	87920	0.00020922
41	112085	0.00027009
42	123436	0.00012737
43	137404	9.6615e-05
44	150259	7.6441e-05

Case 5 used ~ 199K meshes

Number of Passes: Completed 45, Maximum 55, Minimum 1
Max Mag. Delta S: Target 8E-05, Current 7.1117e-05
View: Table / Plot
Export...
CONVERGED
Consecutive Passes: Target 1, Current 1
Default Settings: Save Defaults, Clear Defaults

Pass Number	Solved Elements	Max Mag. Delta S
30	9790	0.0024609
31	12472	0.0021887
32	15834	0.0019169
33	19395	0.0012917
34	24588	0.0010546
35	31226	0.00098709
36	39645	0.00075146
37	48677	0.00058644
38	59977	0.00042192
39	76403	0.00036896
40	86699	0.00020522
41	110441	0.00025916
42	140710	0.00023203
43	160179	0.00013031
44	179374	8.9112e-05
45	199376	7.1117e-05

Summary

- Correlated measured DUT, HFSS and X2D2 using various frequency-dependent DK, DF and roughness models.
  - Showed how to equate effective conductivity to Huray model.
  - Showed different setup conditions with different DK, DF, and roughness model.
- Need many meshes in HFSS to have high accuracy for 2D structures.
  - At least 4 meshes(?) on the larger side of conductor cross section are needed.

Case	Solver	DK/DF model	Roughness model	Delta S	Total # meshes	CPU time (min)
1	HFSS	Tabular DK/DF	Tabular conductivity	0.00008	634254	240
2	HFSS	Tabular DK/DF	Tabular conductivity	0.0003	112323	25
3	HFSS	Tabular DK/DF	Tabular conductivity	0.001	3735	8
4	HFSS	Tabular DK/DF	Huray model	0.00008	150259	30
5	HFSS	Djordjevic-Sarkar	Tabular conductivity	0.00008	199376	50
6	X2D2	Djordjevic-Sarkar	Effective conductivity	n/a	~300	< 5

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- Christer Sevnsson and Gregory E. Dermer, “Time domain modeling of lossy interconnects,” IEEE Tran. On Advanced Packaging, Vol. 24, No. 2, May 2001.
- Djordjevic, R.M. Biljic, V.D. Likar-Smiljanic, T.K.Sarkar, “Wideband Frequency-Domain Characterization of FR-4 and TimeDomain Causality,” IEEE Trans. on EMC, vol. 43, No. 4, November 2001.
- J. Eric Bracken, “A causal Huray model for surface roughness,” DesignCon 2012.
- Gerald Gold and Klaus Helmreich, “A physical surface roughness model and its applications,” IEEE Tran. on Microwave Theory and Techniques, Vol. 65, No. 10, October 2017.
- Dusan N. Grujic, “Closed-form solution of rough conductor surface impedance,” IEEE Trans. On Microwave Theory and Techniques, Vol. 66, No. 11, November 2018.

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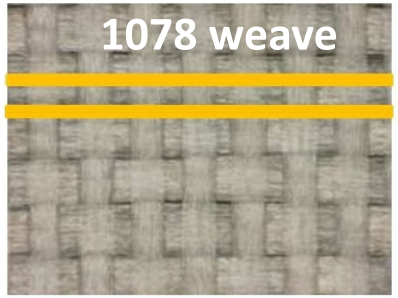
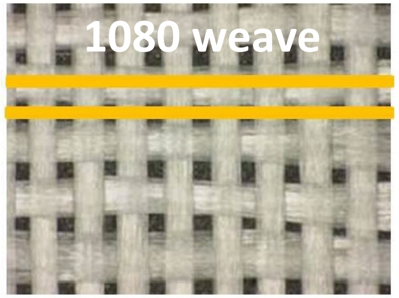
- Summary : Ching Chao Huang

Addressing skew impairments in characterization

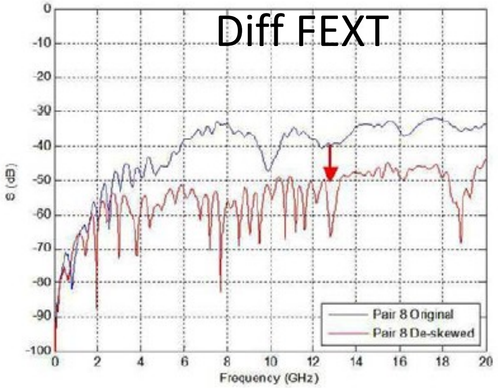
Motivation

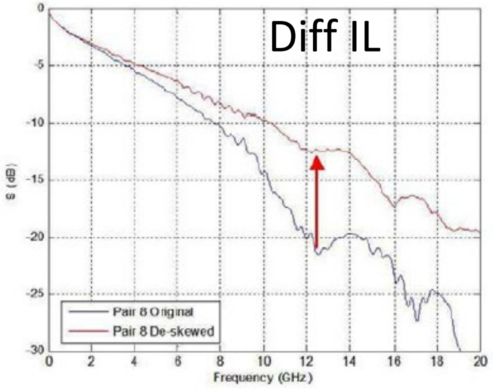
- 1) Fiber weave effect.





30ps skew





- 2) Skew affects Dk/Df extraction.

6” + DUT + 6”

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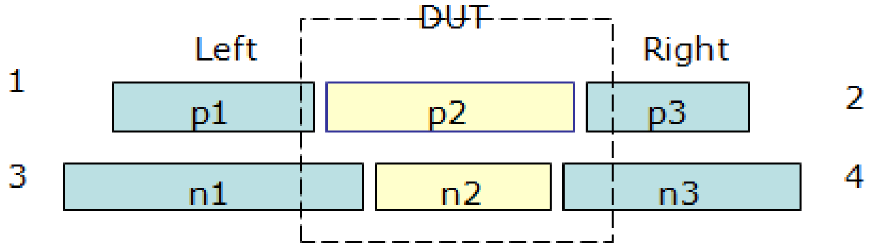
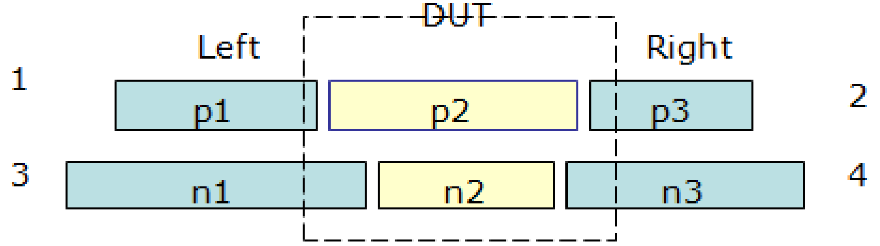
What is skew?

- Delay between p- and n-line: p2-n2.



DUT skew via de-embedding

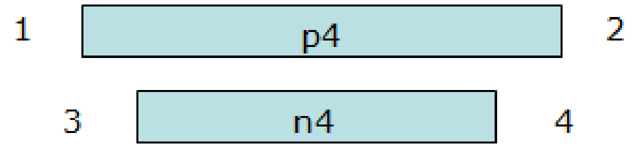
Fixture+DUT



Port 1→2: p1+p2+p3

Port 3→4: n1+n2+n3

2X-thru



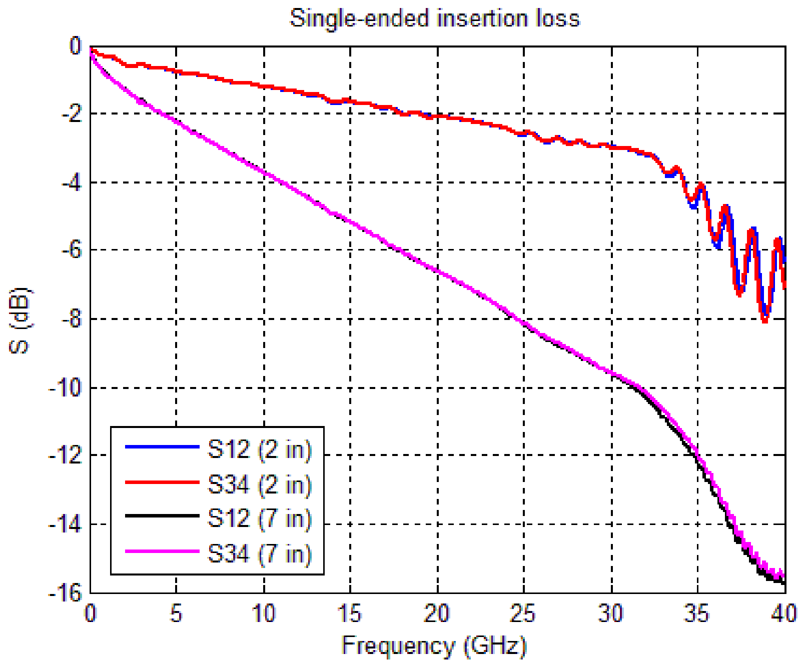
Port 1→2: p4

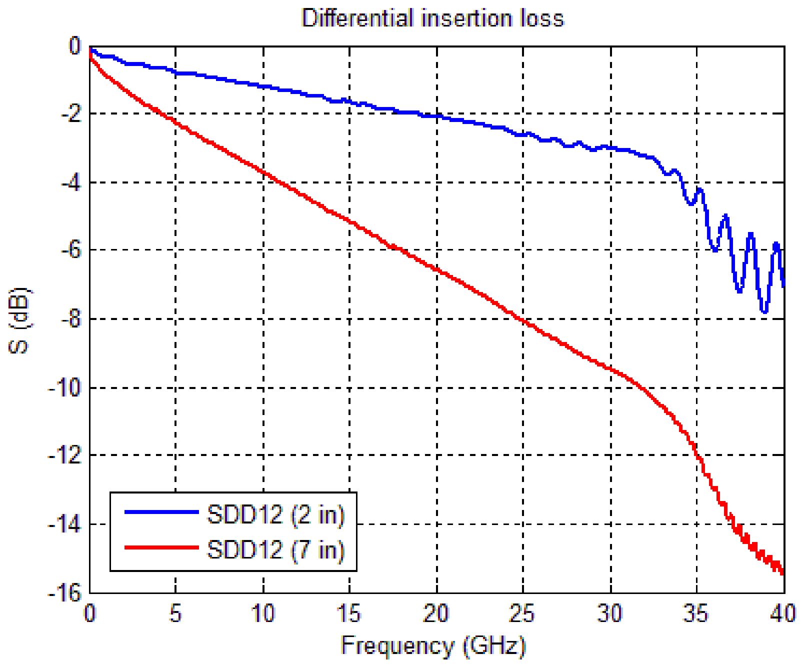
Port 3→4: n4

$$\text{De-embedded skew@DUT} = (p1 + p2 + p3 - p4) - (n1 + n2 + n3 - n4)$$
$$= (p2 - n2) + \big(p1 + p3 - (n1 + n3)\big) - (p4 - n4)$$
$$= Skew@DUT + Skew@Fixture - Skew@Coupon$$

PCB measurement via de-embedding

- Single-ended and differential insertion loss look okay.

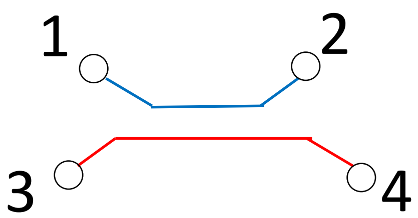




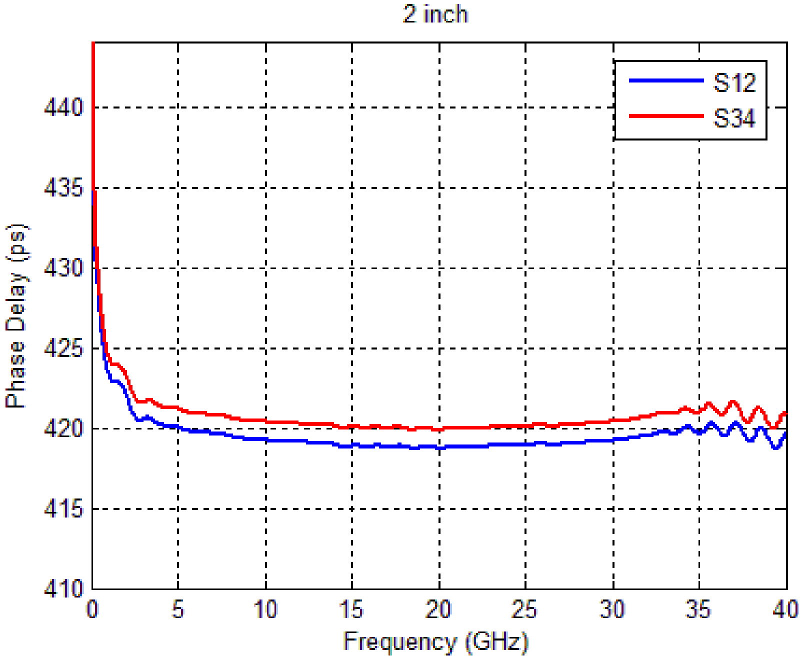
Opposite skew in coupon and fixture + DUT

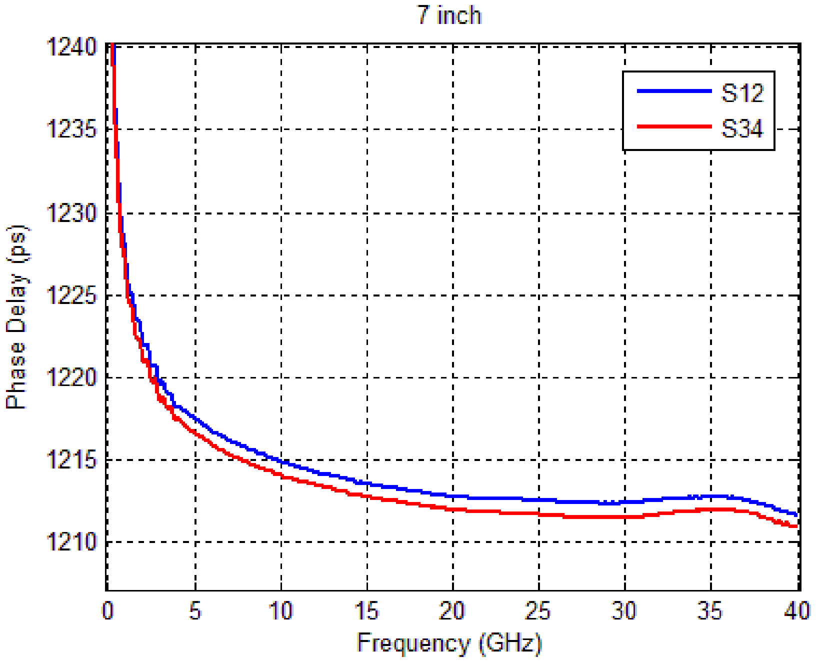
- With 5ps rise time (20/80),
  - 2” gives -1.1584 ps skew.
  - 7” gives 0.909807ps skew.

2” structure



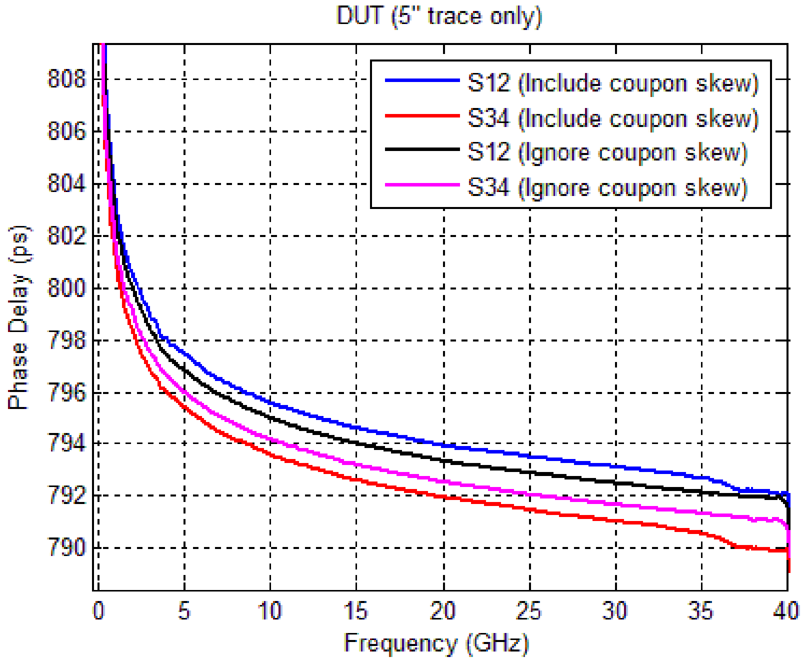
7” structure

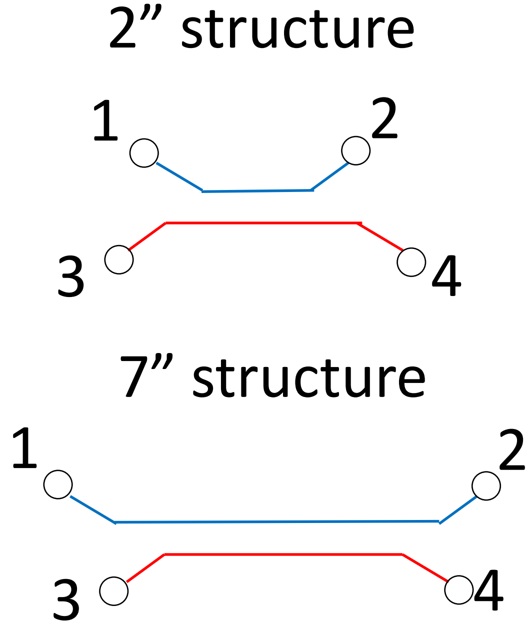




De-embedded result

- Include coupon skew in de-embedding gives more skew.
- DUT with more skew (include coupon skew in this case) results in more insertion

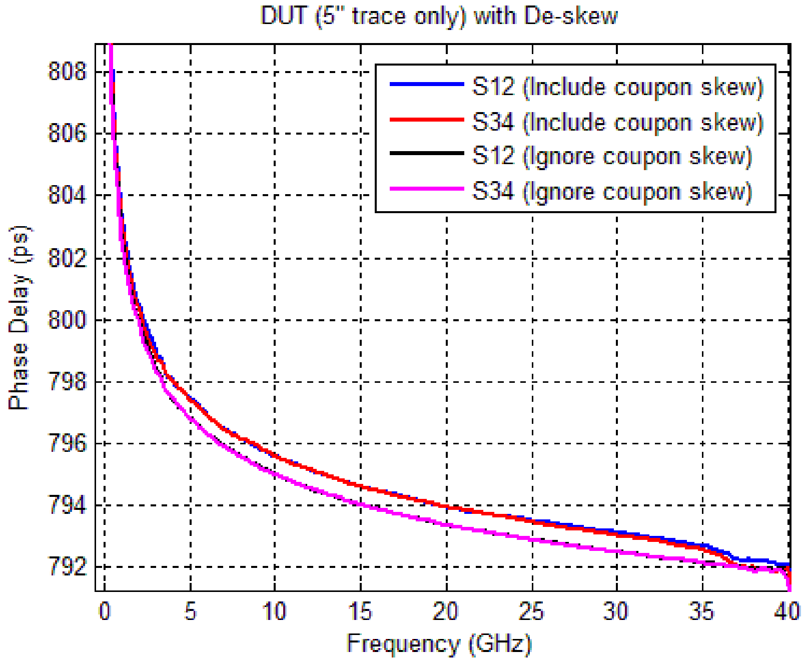


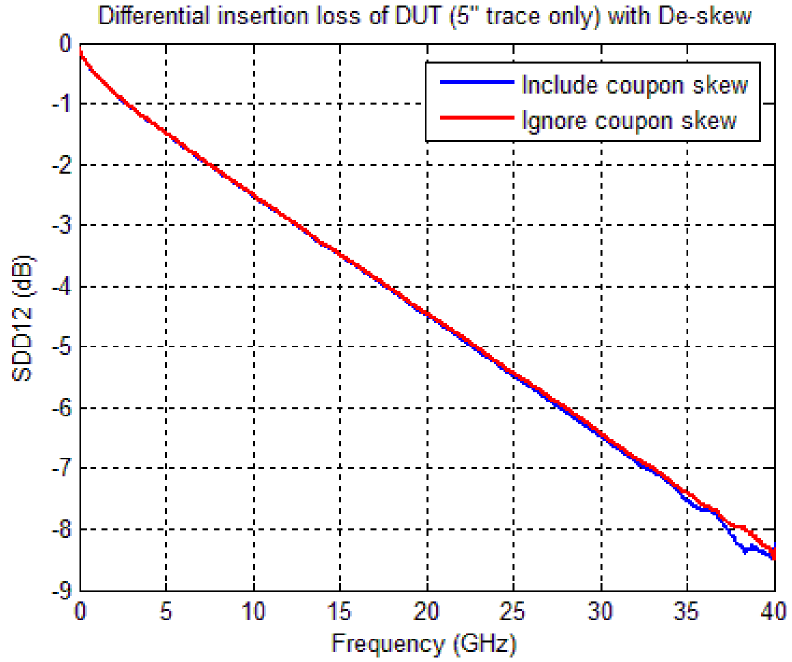


Include coupon skew: Each coupon trace delay is used for de-embedding.
Ignore coupon skew: Average coupon trace delay is used for de-embedding. Therefore, ***NO*** coupon skew.

De-skew for unbiased 'loss per inch'

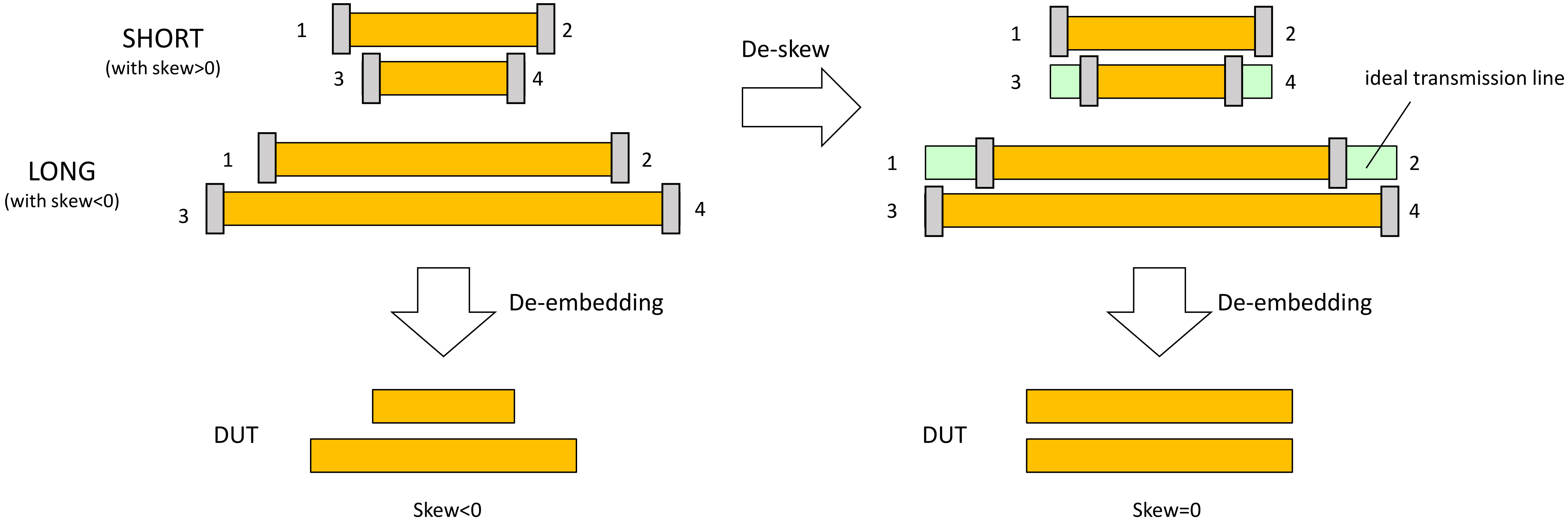
- Padding ideal T-line to shorter trace to match phase delay of longer trace.
- A more consistent differential insertion loss ➔ unbiased 'loss per inch'.





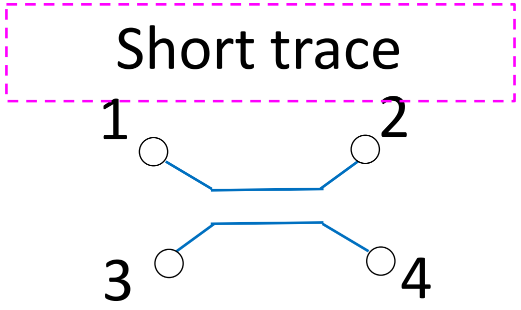
Skewless de-embedding

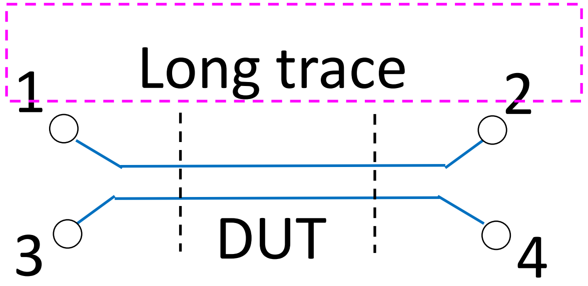
- Pad ideal transmission line to de-skew.



DUT skew is worse when long and short diff pairs have opposite skew.

Quick review of eigenvalue solution (Delta-L)





Assumption:

- DUT is an ideal T-line.
- Identical launches.

$$T_1 = T_A * T_B \qquad T_2 = T_A * T_{DUT} * T_B \;\Rightarrow\; T_2 * {T_1}^{-1} = T_A * T_{DUT} * {T_A}^{-1}$$

Diagonalize $T_{DUT} = P * \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{pmatrix} * P^{-1}$

Observation: T_{DUT} and $T_2 * {T_1}^{-1}$ share the same eigenvalue

Let $T_2 * {T_1}^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix}$

$$e^{-\gamma l} = \frac{(a+d) \pm \sqrt{(a-d)^2 + 4bc}}{2}$$

eigenvalue

Modal propagation constant

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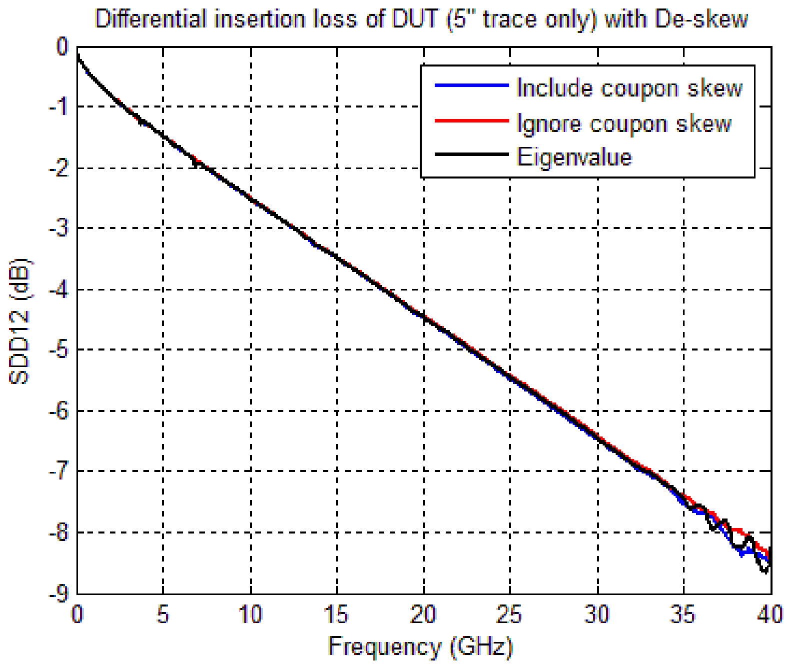
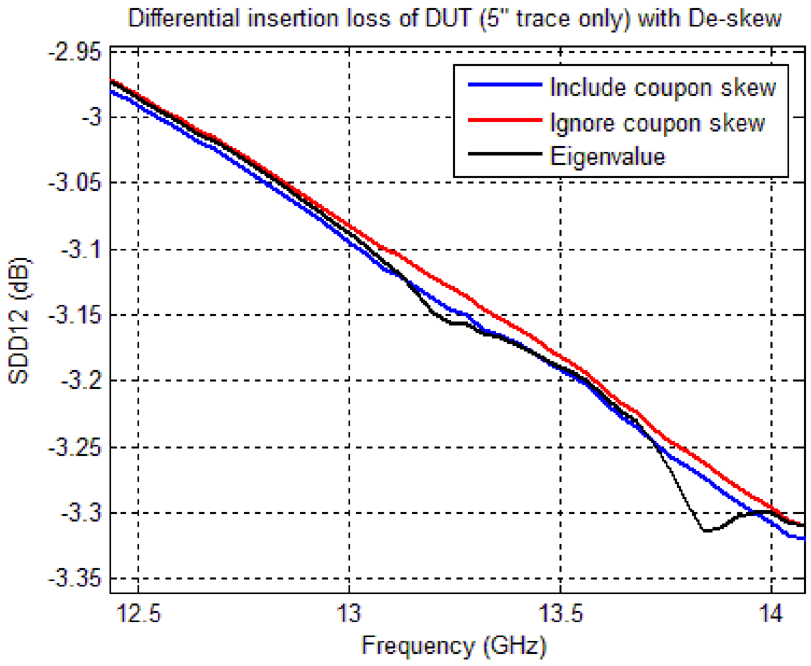
Eigenvalue vs. DUT

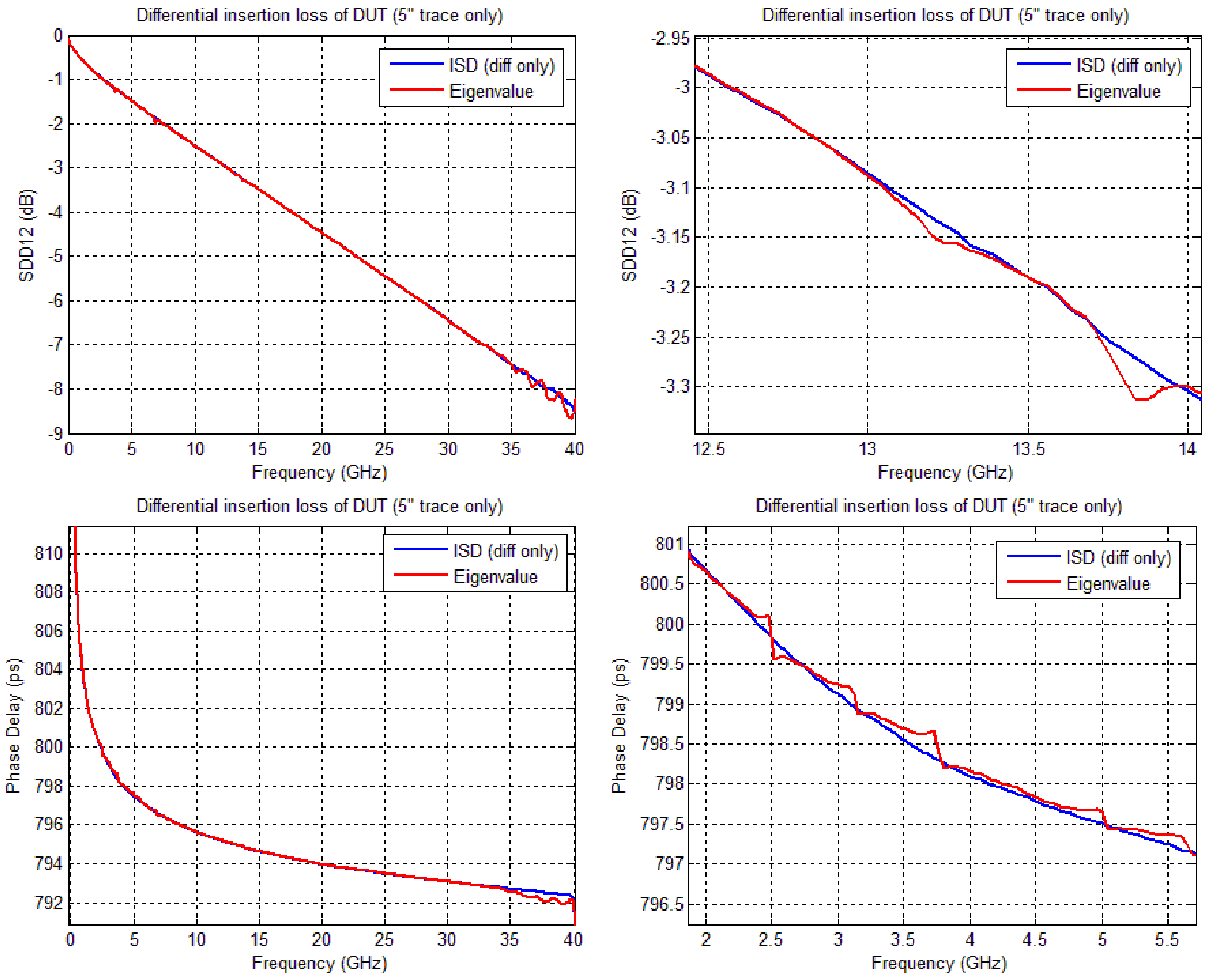
- Eigenvalue solution operates directly on differential (or common) mode only.
  - It has no information of DUT skew.
- Glitches and spikes in eigenvalue solution.
  - Due to assumption of ideal T-line and identical launches.



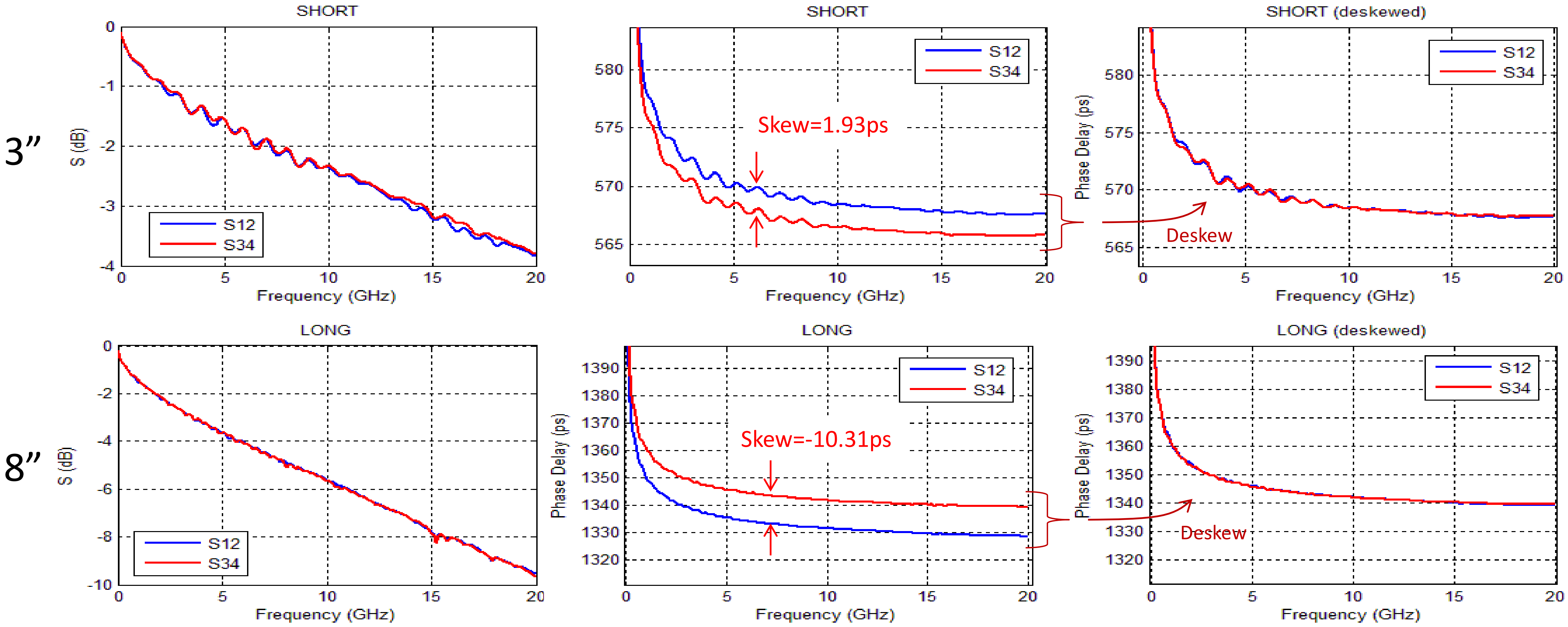


Eigenvalue vs. ISD*

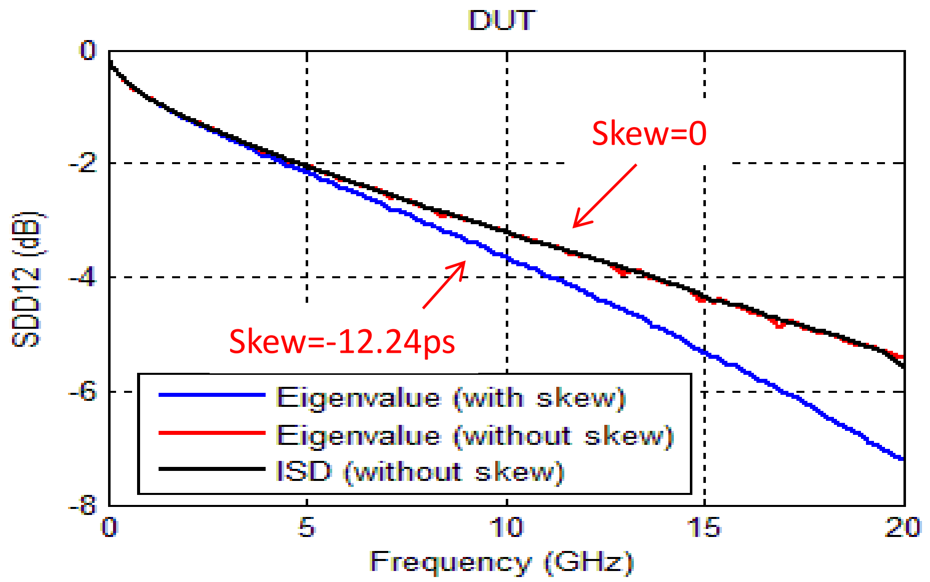
- Use ISD to de-embed differential mode and compare with eigenvalue.
- ISD does not give glitches and spikes.
- ISD does not assume identical launches or uniform T-line for DUT.

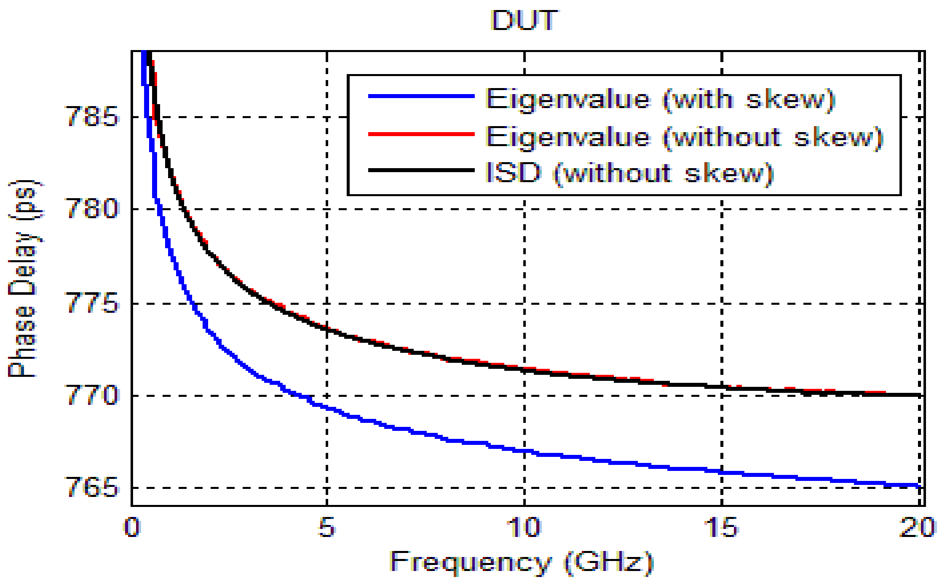


Example 2: De-skew 3" and 8" pairs before de-embedding



Skew affects de-embedded results (and therefore DK/DF/SR extraction)





Takeaways

- Fiber weave effect may contribute to PCB skew.
- Fixtures and DUT skews are unknow. It is difficult to quantify skew by de-embedding.
  - When fixture and coupon have opposite skew, de-embedding gives more DUT skew.
- De-skewed de-embedding gives unbiased insertion loss and therefore accurate extracted Dk/Df/SR.

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- A. Nagao, T. Takada, C.C. Huang, J. Buan, K. Aihara, "New methodology for 25+ Gbps connector performance characterization", DesignCon 2014, Santa Clara, CA
- J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, "Aristotle: A fully automated SI platform for PCB material characterization," DesignCon 2017, Santa Clara, CA.
- C. Luk, J. Buan, T. Ohshida, P.J. Wang, Y. Oryu, C.C. Huang and N. Jarvis, "Hacking skew measurement," DesignCon 2018, Santa Clara, CA.

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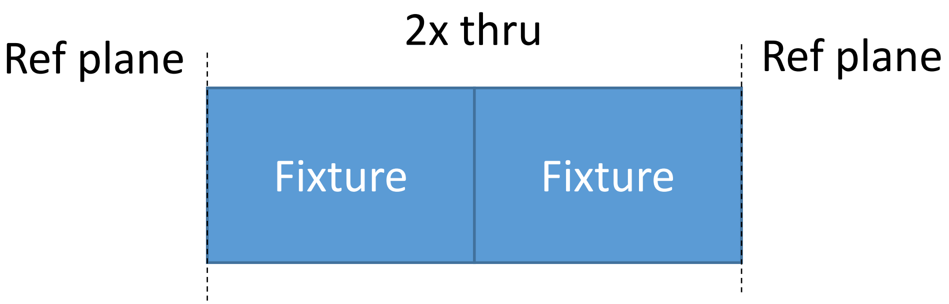
Test Fixture Design

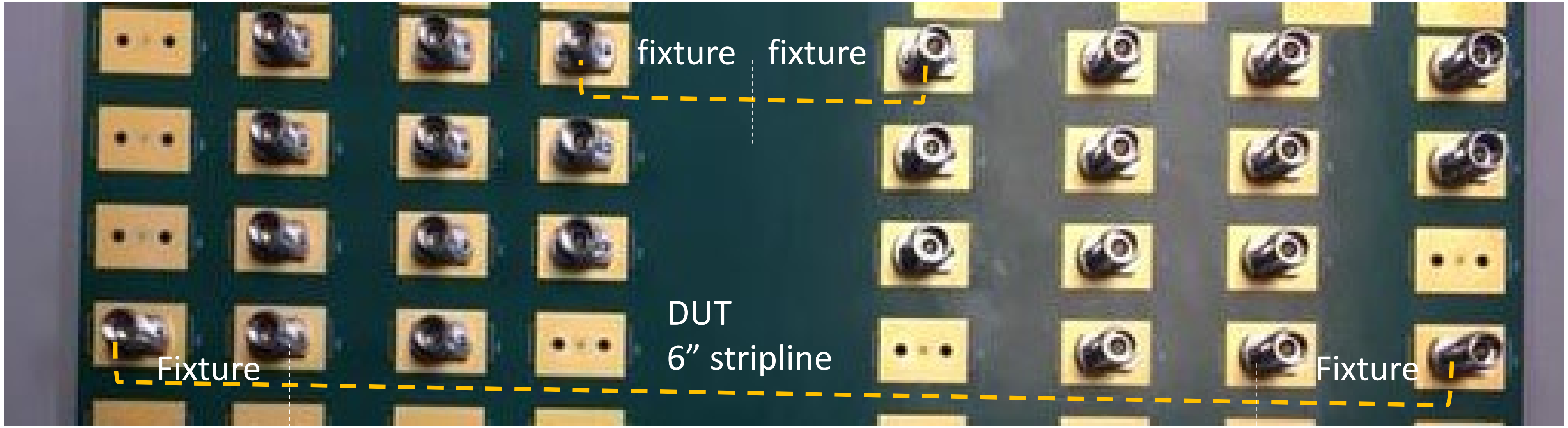
Outline

- Bandwidth consideration for test fixture design
- Example test fixture
- Fixture design studies
  - Connector and probe study
  - Fixtureless extraction study
- Test fixture design summary

Bandwidth consideration for test fixture design

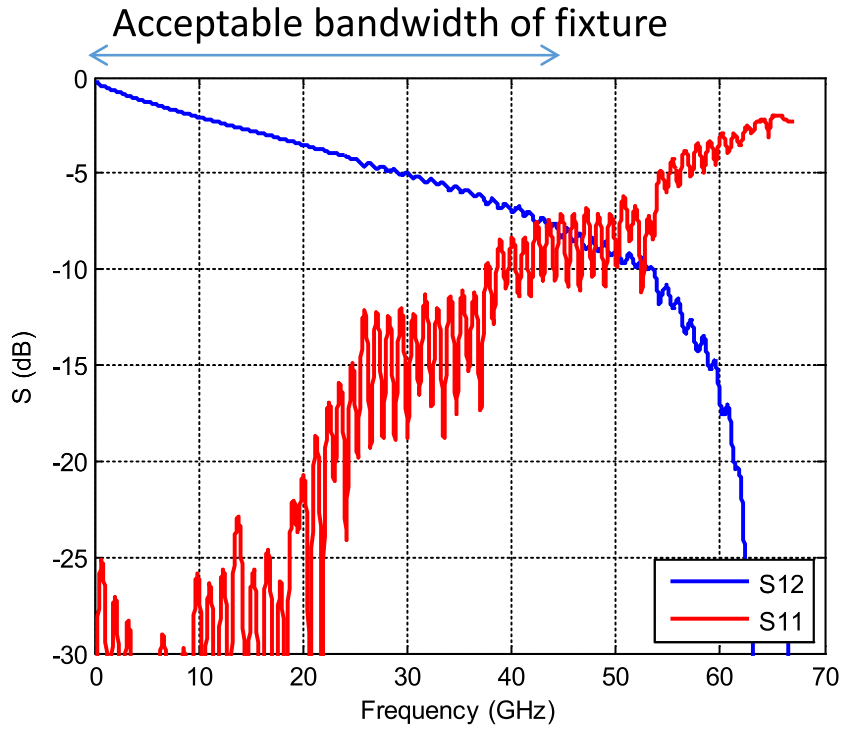
DUT, fixture, and 2x thru





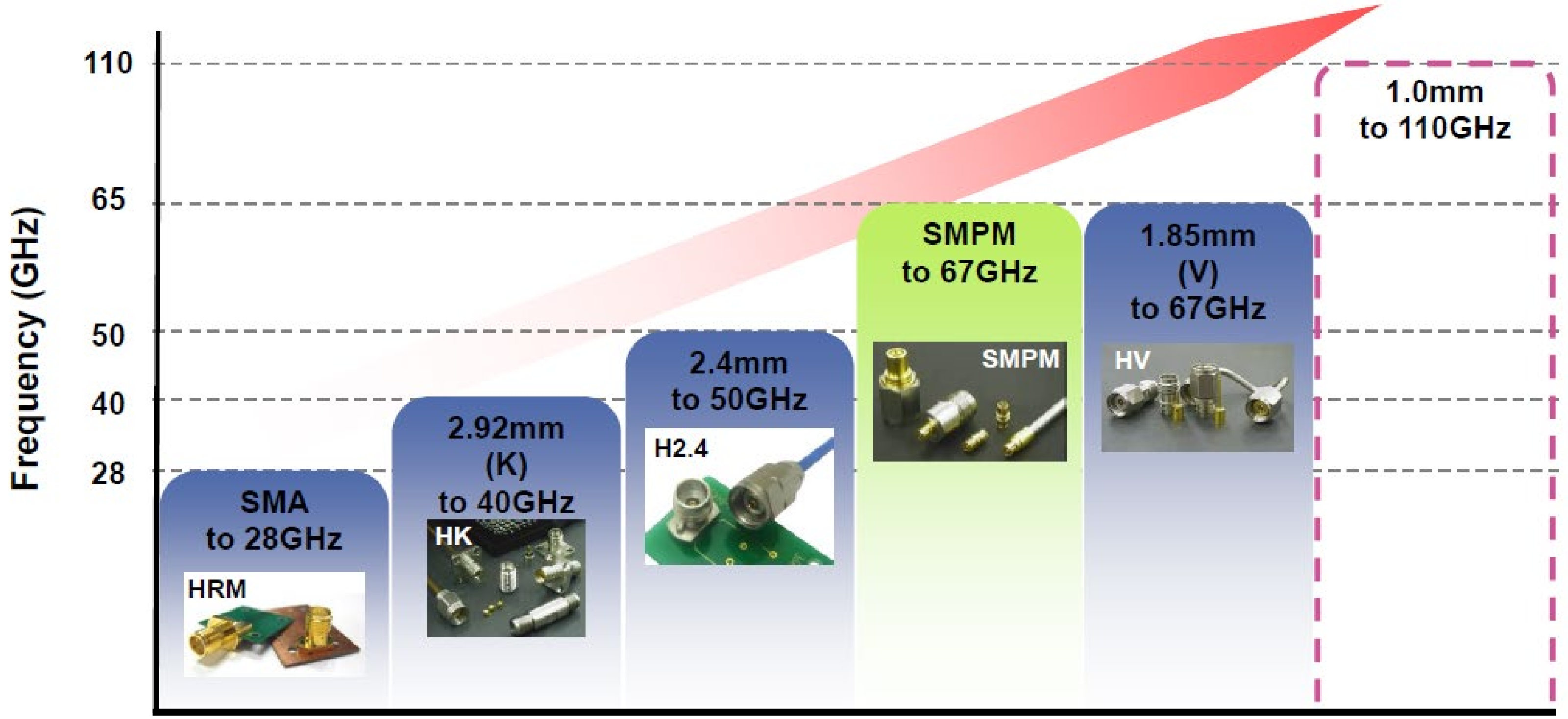
2x thru requirements

- As a rule of thumb, the insertion loss and return loss should not cross up to the frequency of interest.
- Insertion loss should be resonance free up to the frequency of interest.



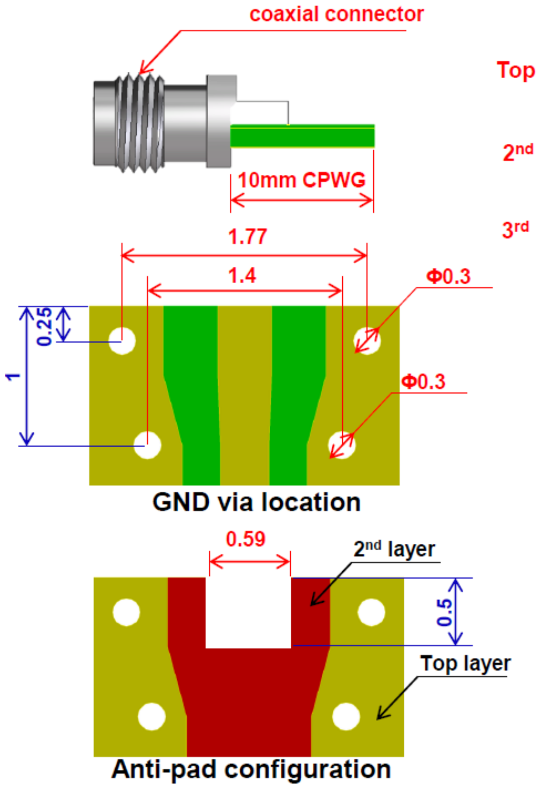
2x thru - Connector consideration

- All coaxial connectors will resonate at some frequency and have impedance discontinuities
- Choose a connector appropriate for your frequency range of interest.



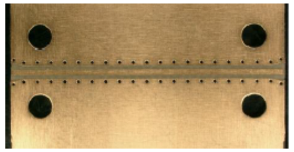
2x thru - Connector footprint consideration

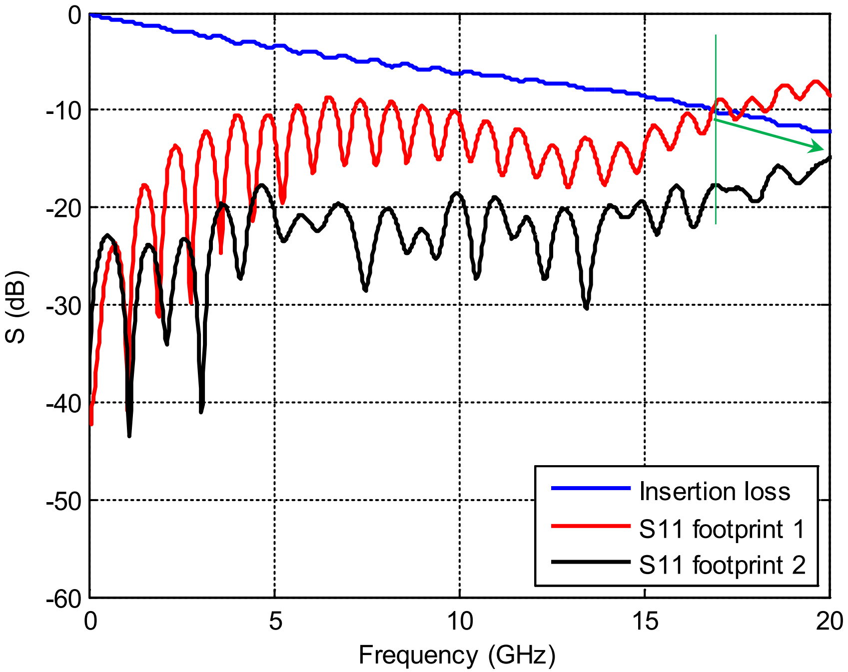
- Even when using the appropriate connector, a bad footprint design can cause large impedance discontinuities, which causes high RL.



PCB stackup

Top	43 micron (Copper foil + Plating)
	200 micronl (FR4 ε_r=4.2)
2nd	18 micron (Copper)
	200 micronl (FR4 ε_r=4.2)
3rd	43 micron (Copper + Plating)

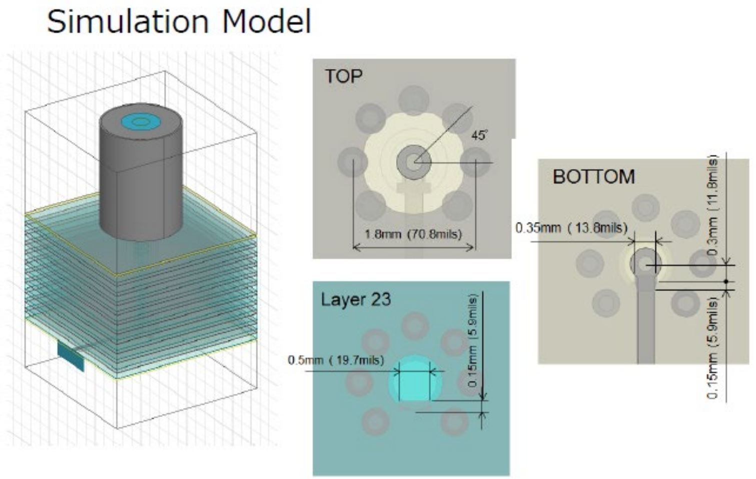


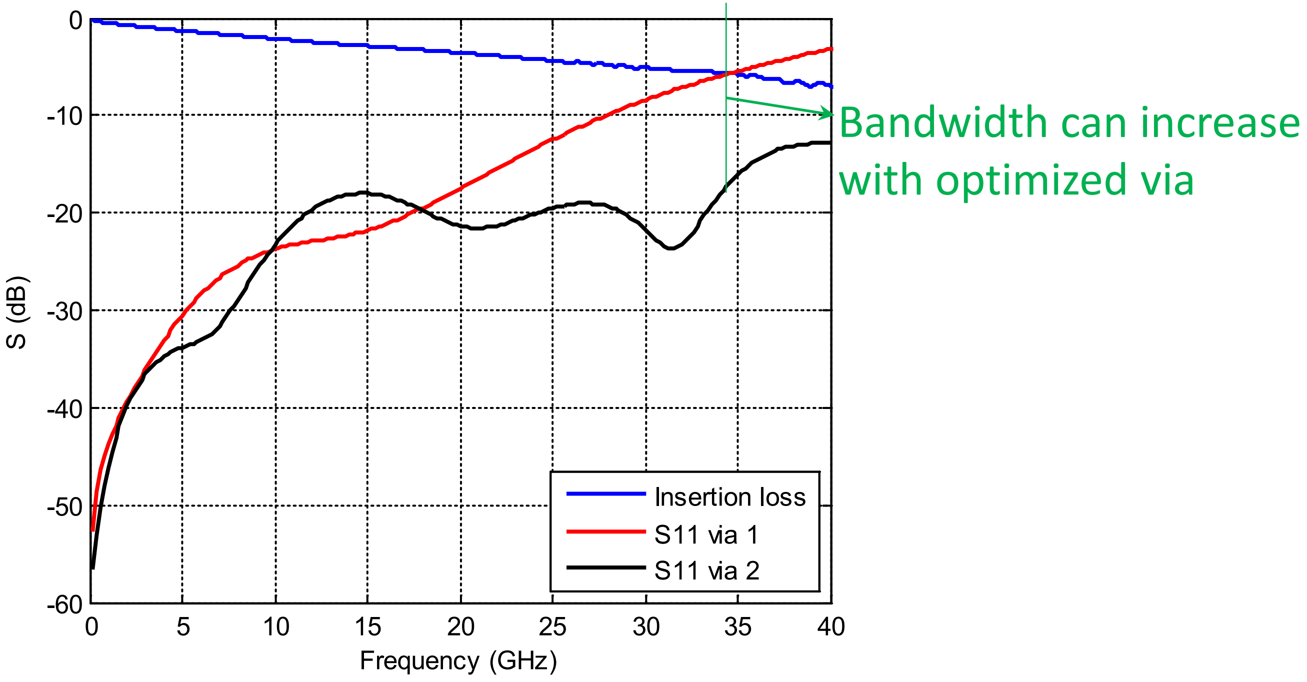


Bandwidth can increase with optimized footrpint

2x thru - Via consideration

- Similarly, poorly designed vias can exhibit large impedance discontinuities.
- Via features to consider
  - Via sizes
  - Gnd via locations
  - Gnd plane antipad sizes/shapes
  - Via stub
  - Pad sizes/shapes





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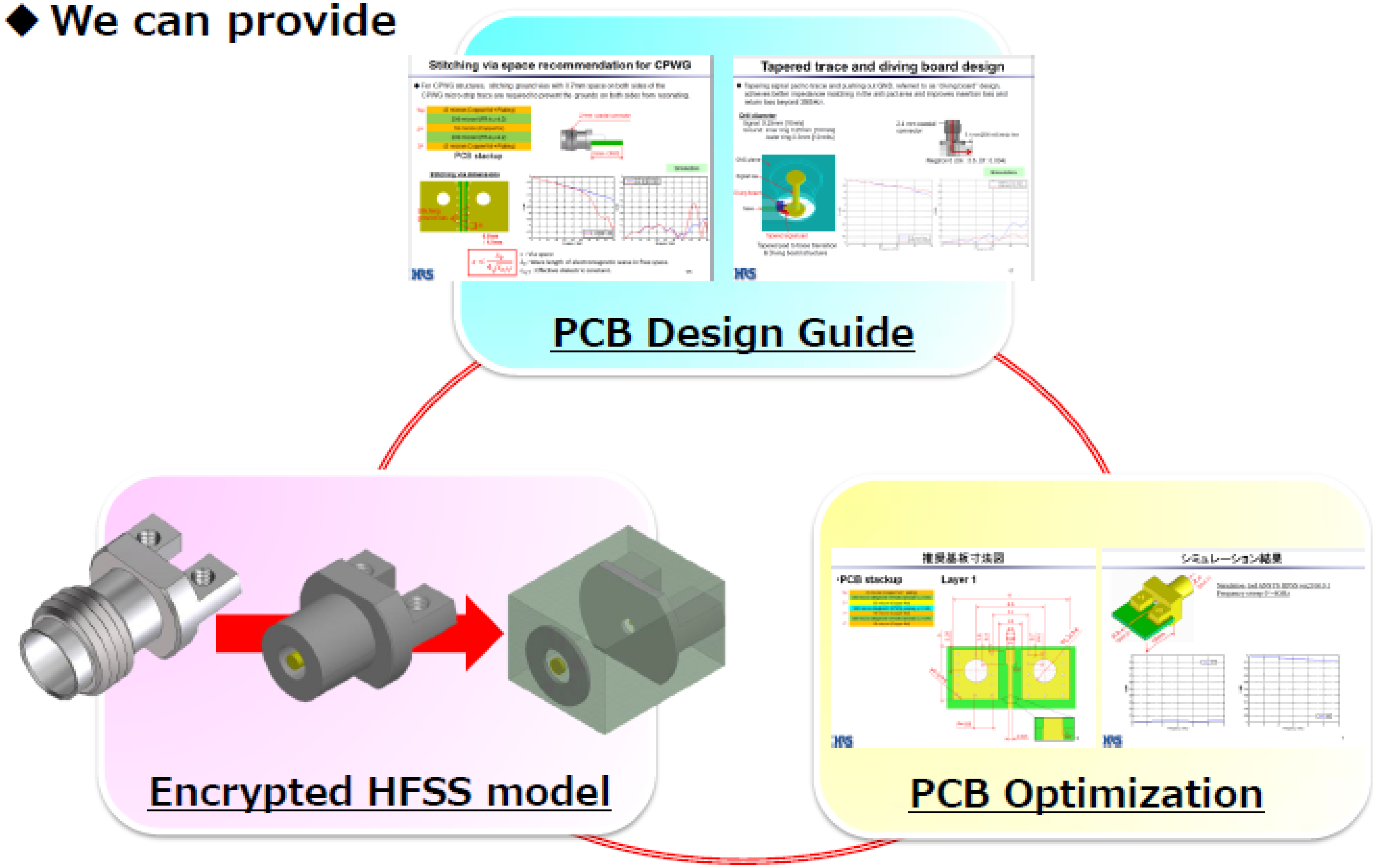
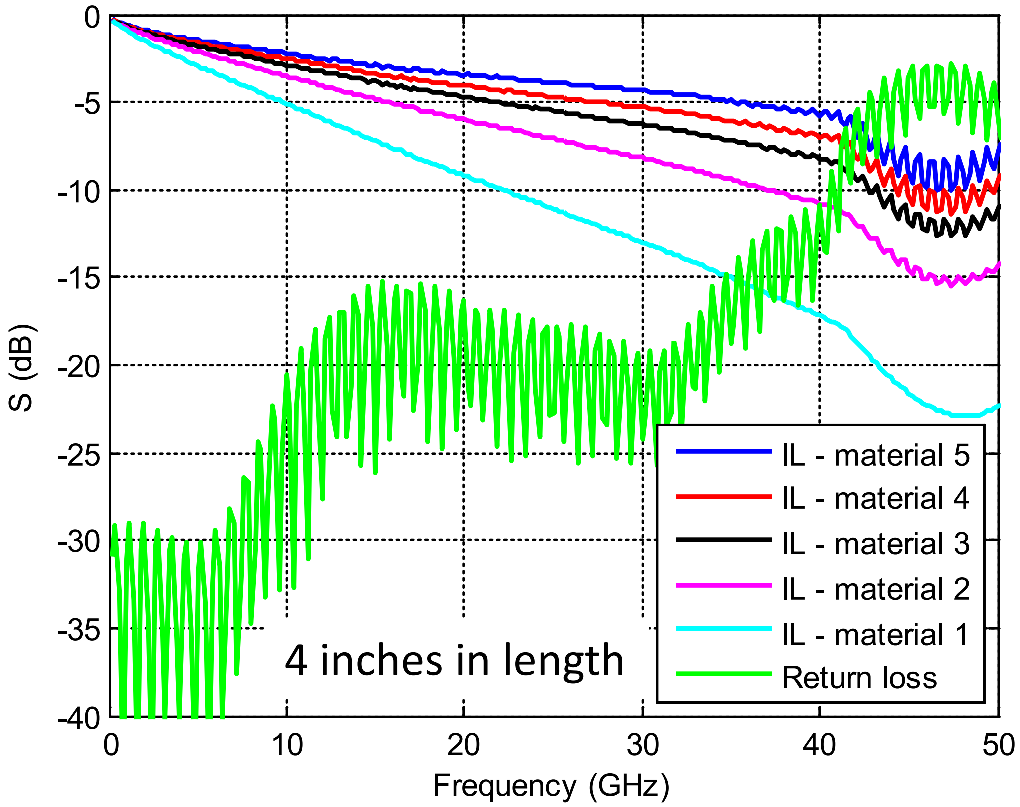
Hirose's PCB Design Support

◆ We can provide



2x thru - PCB material loss consideration

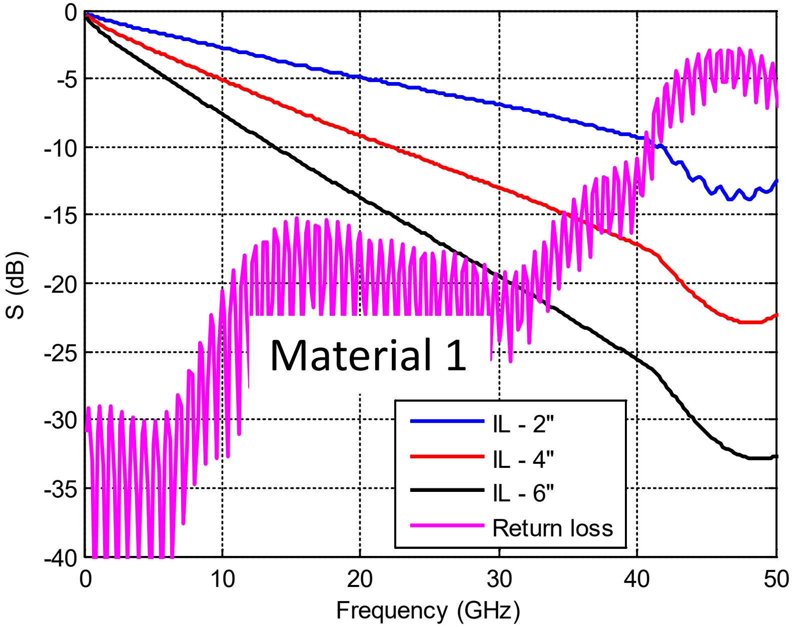
- The bulk of the loss of a fixture typically comes from the PCB trace.
- For a given length, different materials will yield different amounts of loss, which can affect bandwidth



DesignCon 2019 WHERE THE CHIP MEETS THE BOARD

2x thru - PCB trace length consideration

- Similarly, for a given material, different lengths will yield different amounts of loss, which can affect bandwidth
- In this case, 2” is a maximum length to achieve 40GHz bandwidth.



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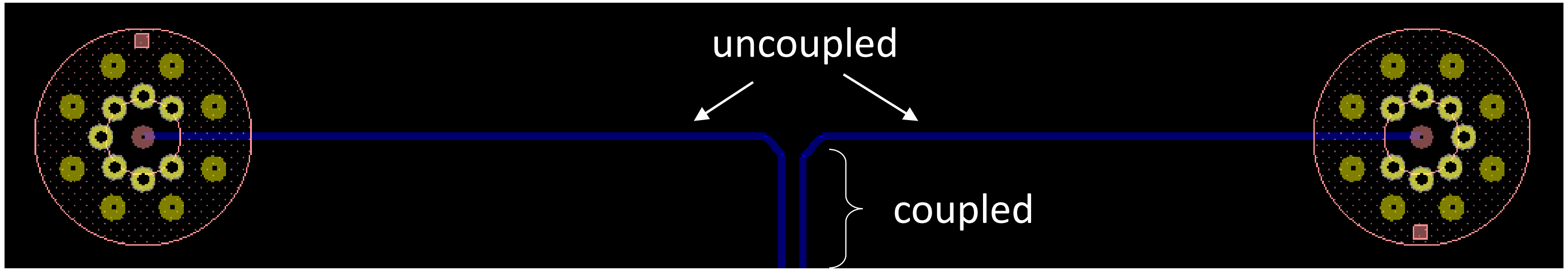
Differential fixture considerations

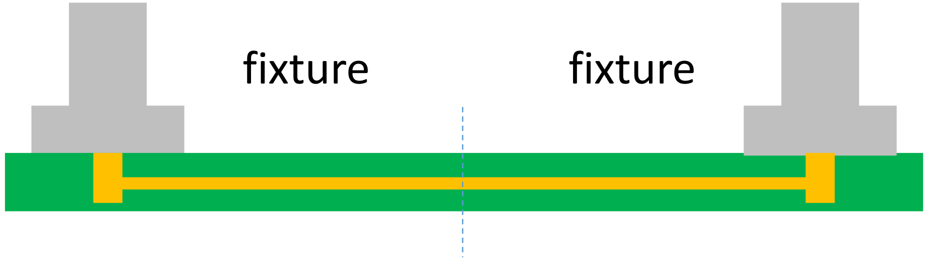
- Skew mitigation
  - Intra-pair skew can affect loss measurements
  - Match lengths of the two lines in layout (1mils max difference is not difficult, which comes out to be <0.2ps on material with Dk=4)
- Connector breakout routing
  - Routing from coupled differential lines to the connectors may require the lines to split and become uncoupled
  - For impedance matching, trace width will need to change at the transition from coupled to uncoupled.

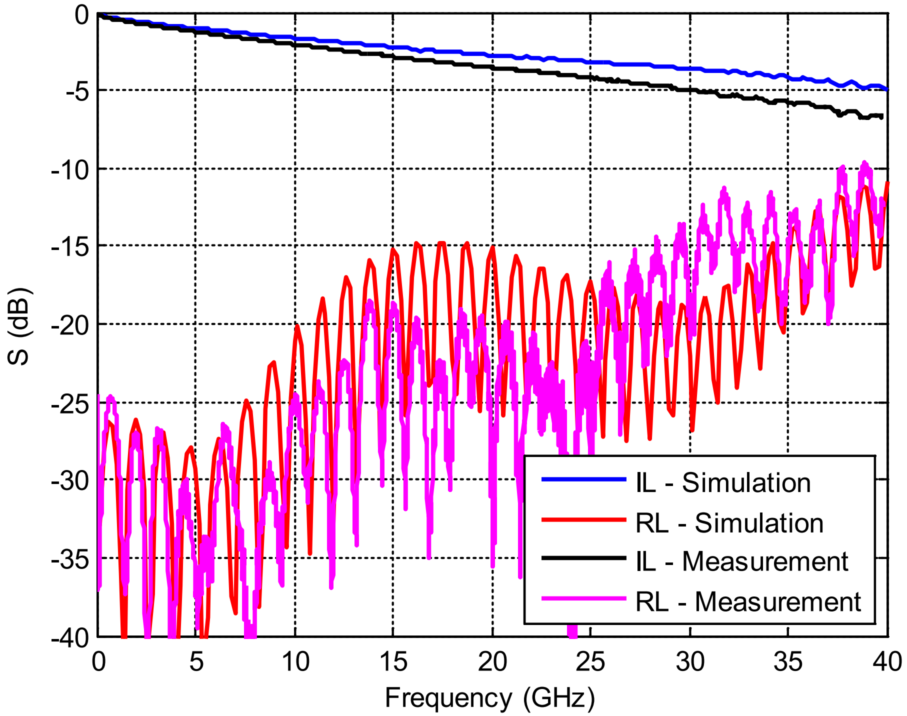


Example test fixture

2x thru fixture-fixture measurement results

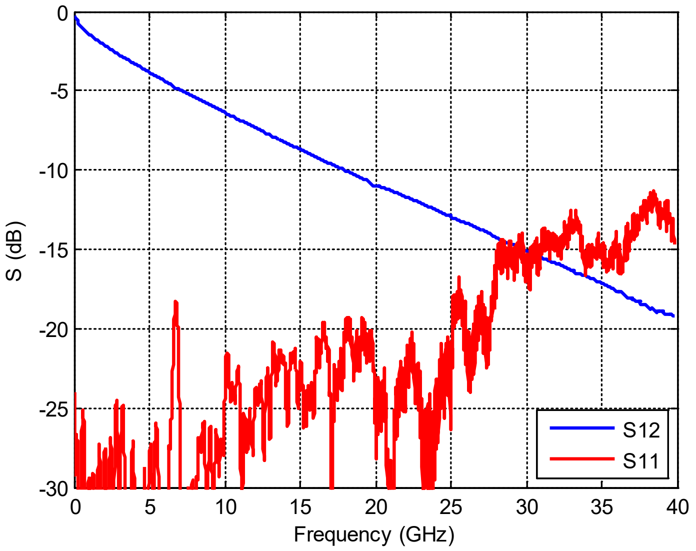
- Comparing the measurement to simulation, measurement shows 1.7dB more loss at 40GHz and 1.5dB higher RL at 40GHz.
- Because there was margin in simulation, measured IL and RL do not cross up to 40GHz. We should be able to get good de-embedded results.



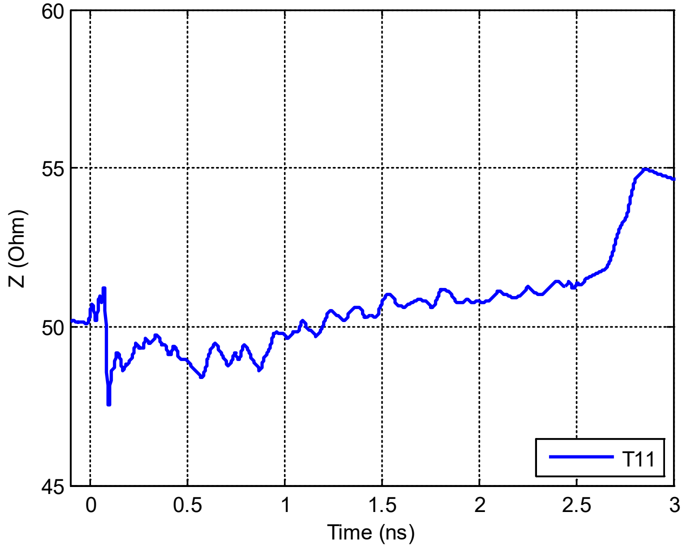


Fixture-DUT-fixture measurement

- IL and RL cross within the bandwidth, but this won't affect the de-embedding quality.

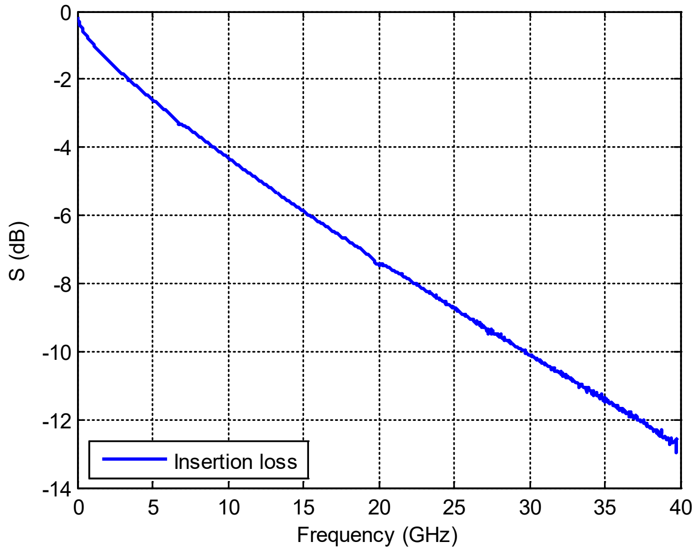


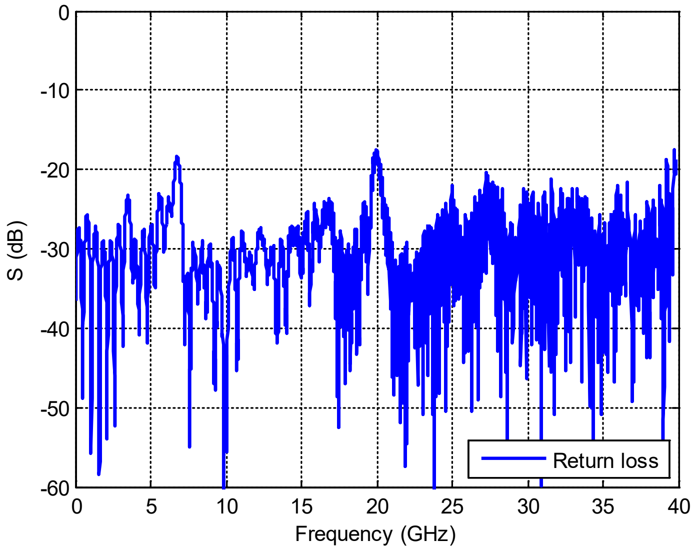
TDR @15ps Trise (20-80)



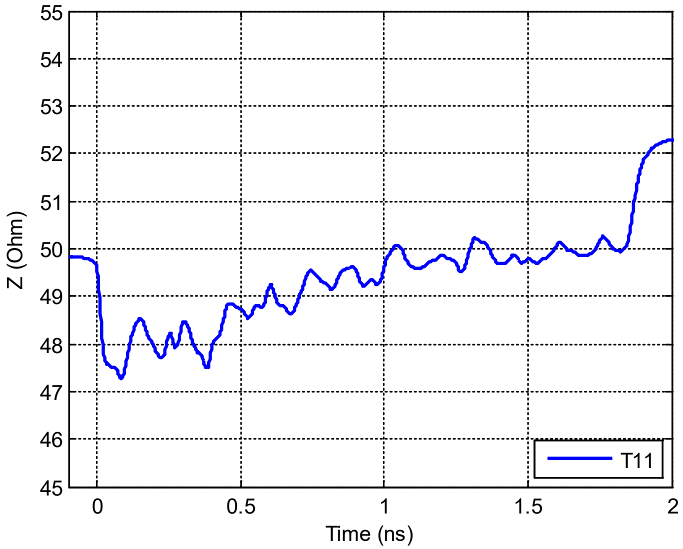
DUT measurement (de-embed by ISD)

- The relative flatness of the RL is evidence that the connector and via are de-embedded.





TDR @15ps Trise (20-80)

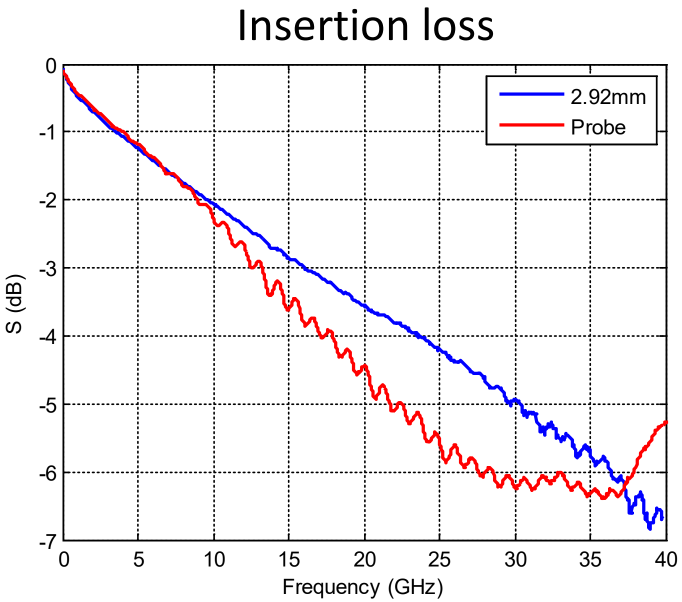


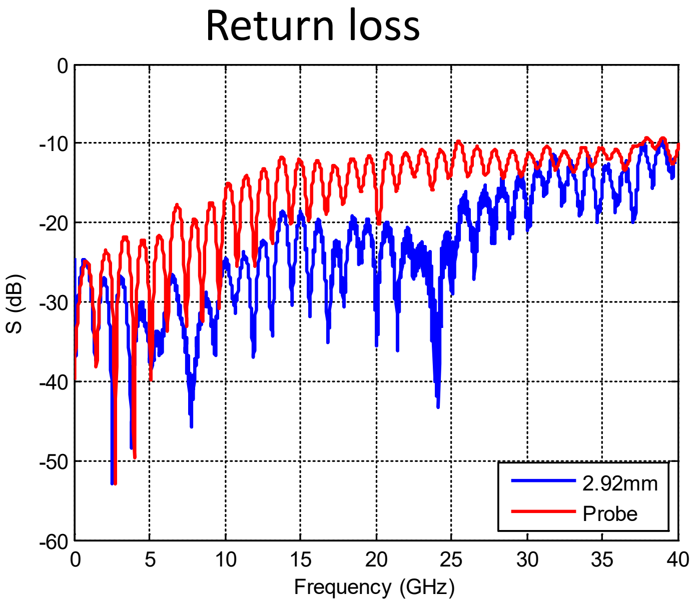
Probe study

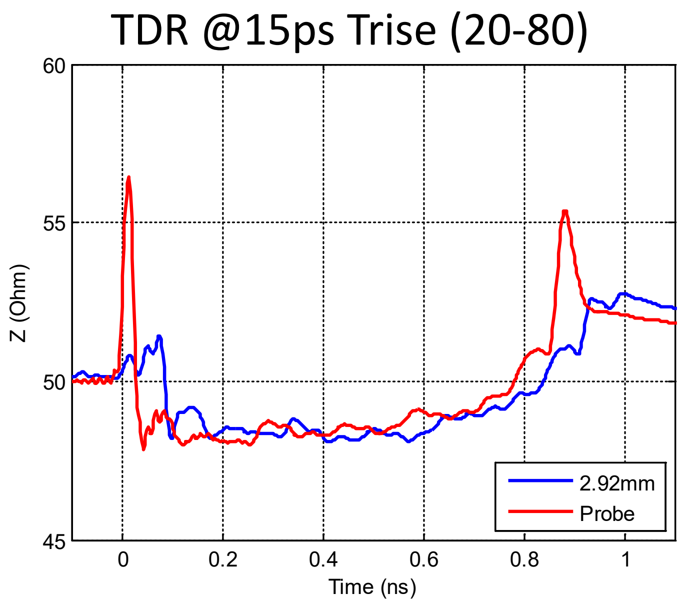
- Objective: To study the feasibility of using probes for characterizing PCB materials.
- DUT: 6” single-ended stripline (same DUT previously shown)
- Fixture: Same PCB as previously shown.
- VNA was calibrated to the tips of the probes.

Fixture-fixture measurements

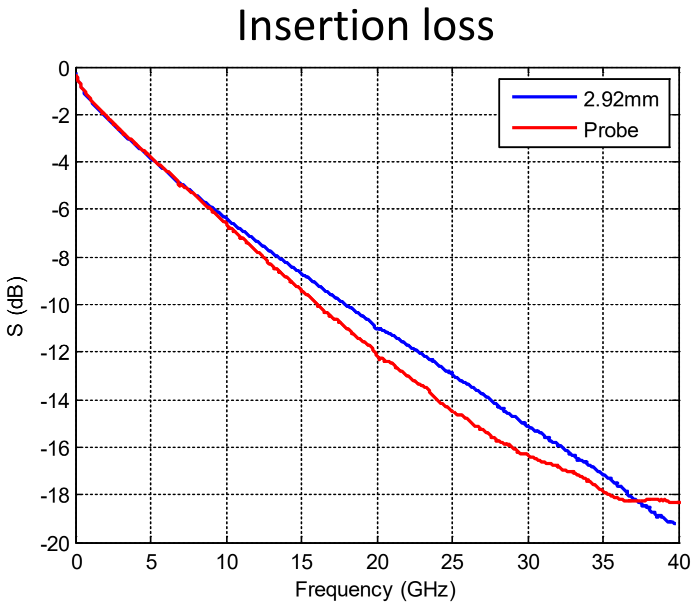
- Probe measurement shows more IL deviation, higher return loss, and larger impedance discontinuities at PCB interface.
- However, it should yield good de-embedding results because IL doesn't cross RL.

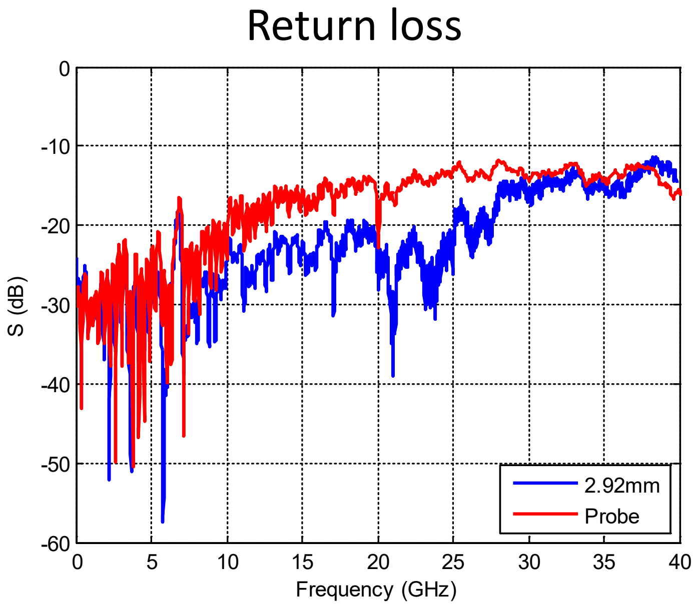


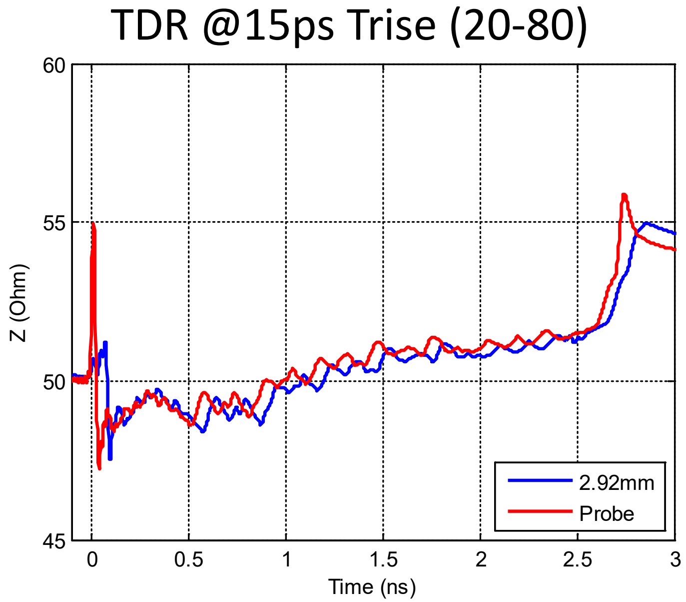




Fixture-DUT-fixture measurements

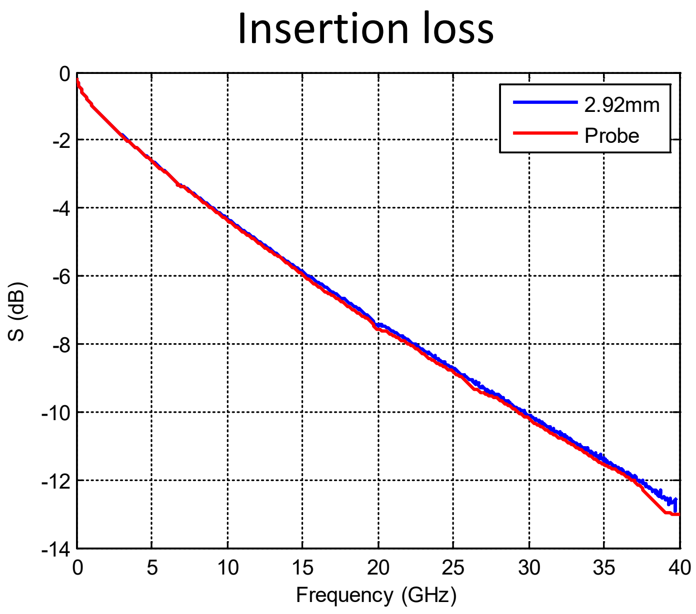


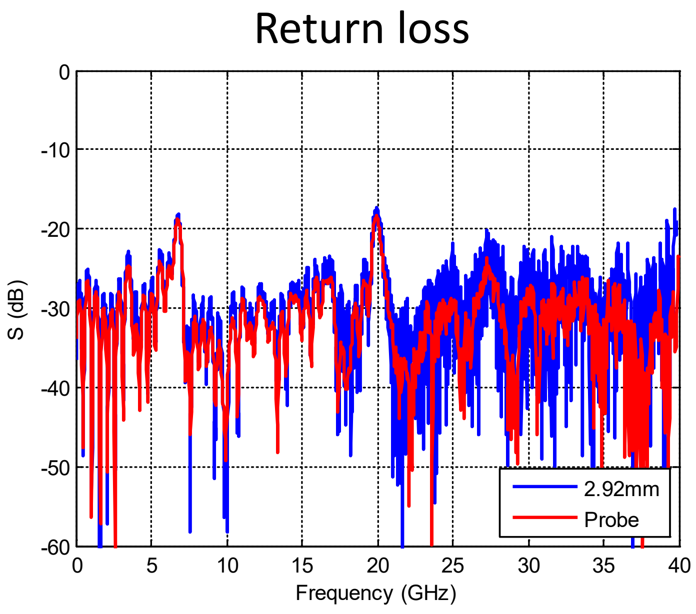


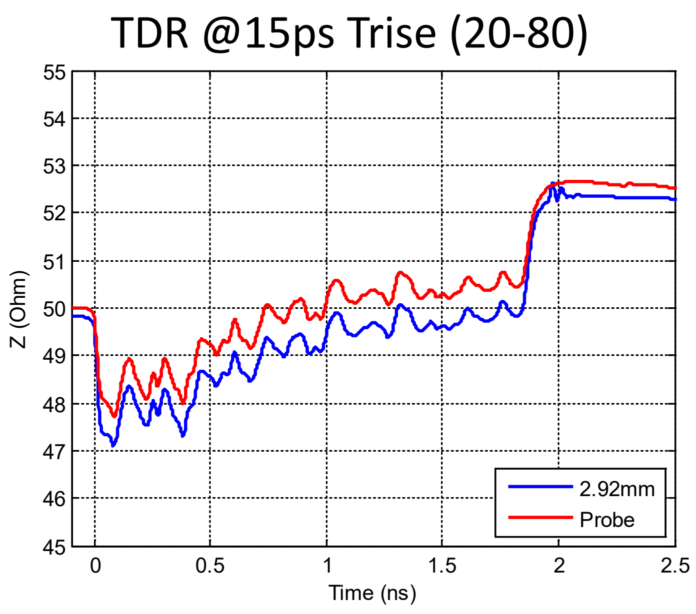


DUT (de-embed by ISD)

- De-embedded DUT measurement results show good correlation, with probe measurement having slightly more loss, slightly lower RL, and slightly higher impedance.



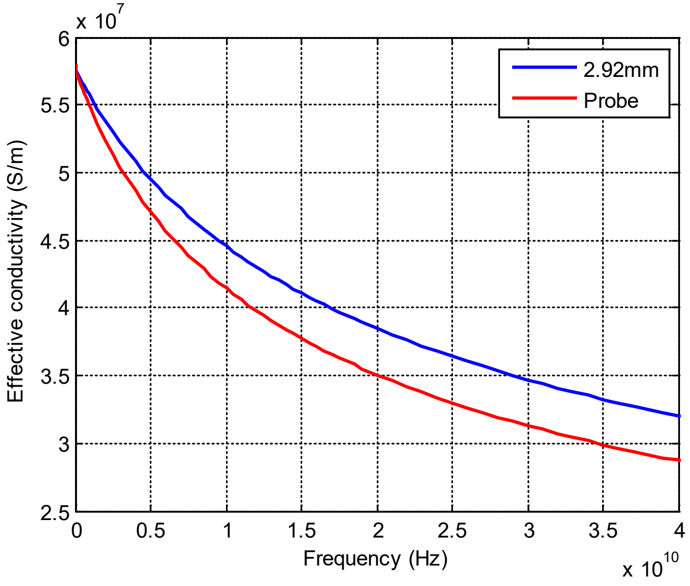


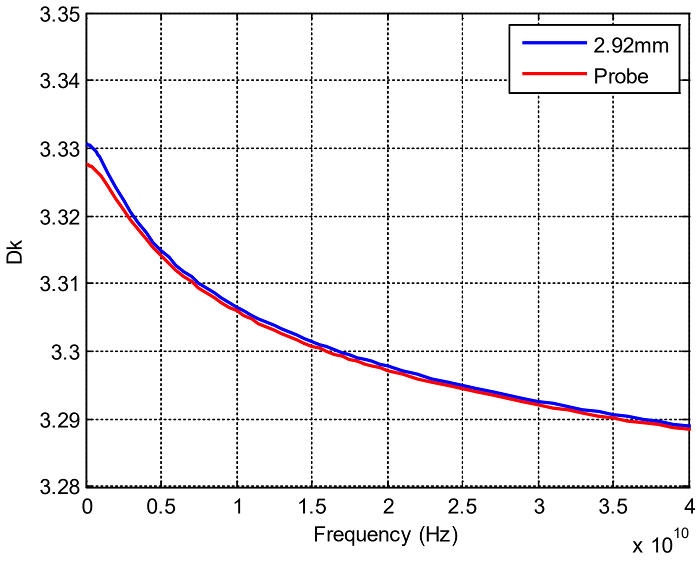


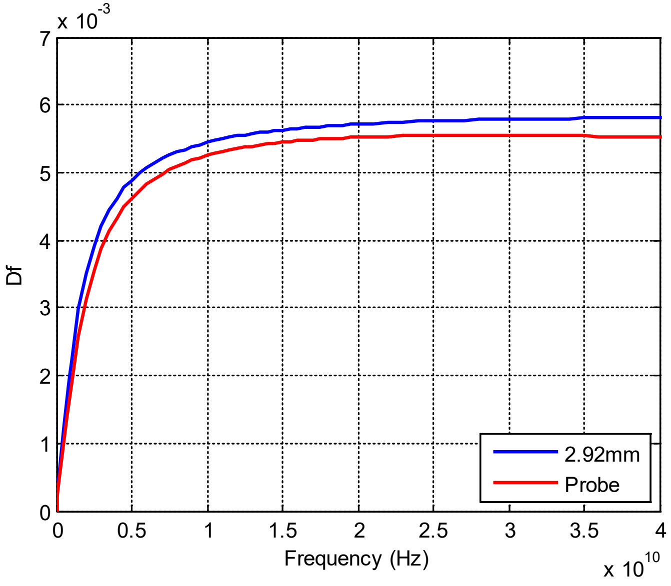
DESIGNCON 2019 WHERE THE CHIP MEETS THE BOARD

MPX extraction with fixed dielectric thickness

- Probe measurement extracted conductivity is ~10% lower and Df is ~5% lower than the 2.92mm measurement.
- Differences may be due to slight difference in de-embedded IL.

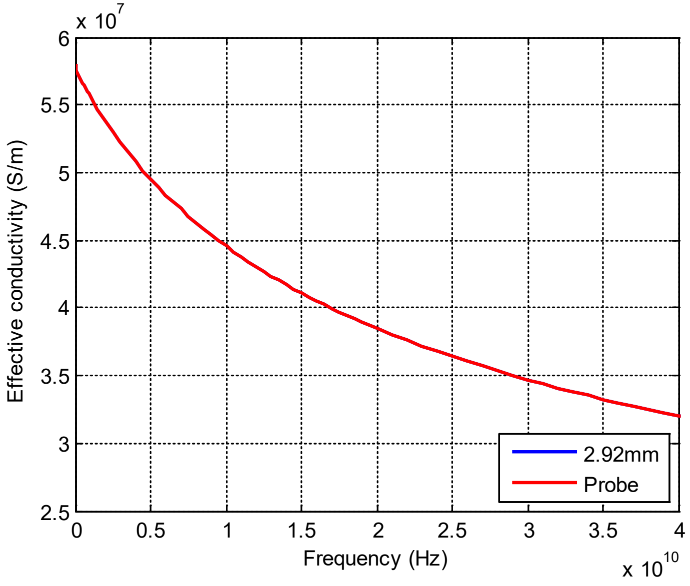


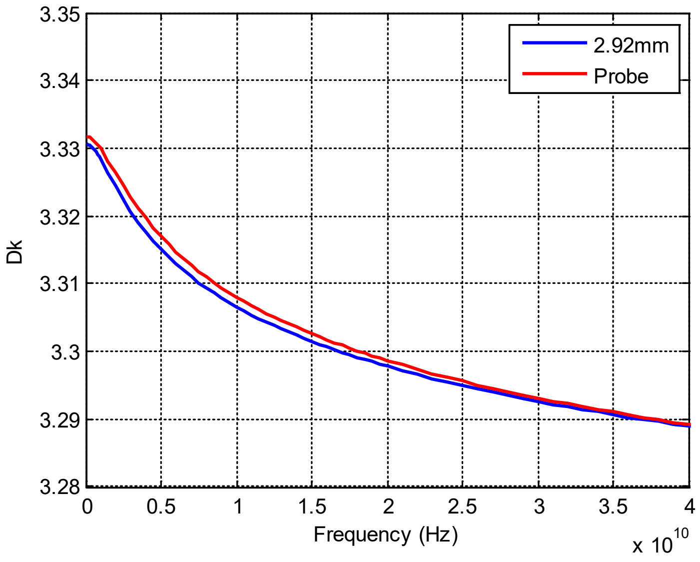


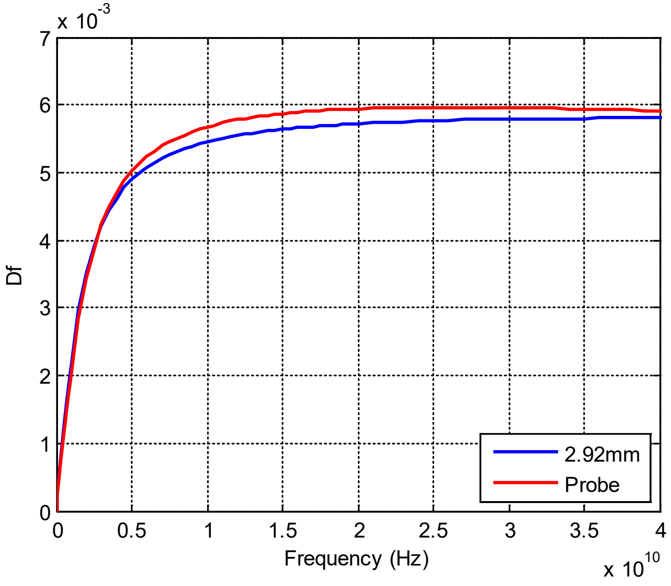


MPX extraction with fixed dielectric thickness, trace width, and Rq

- By fixing dielectric thickness, trace width, and Rq to the measured values, we are able to extract more consistent parameters between the two cases.
- Difference is within 5% for Df.







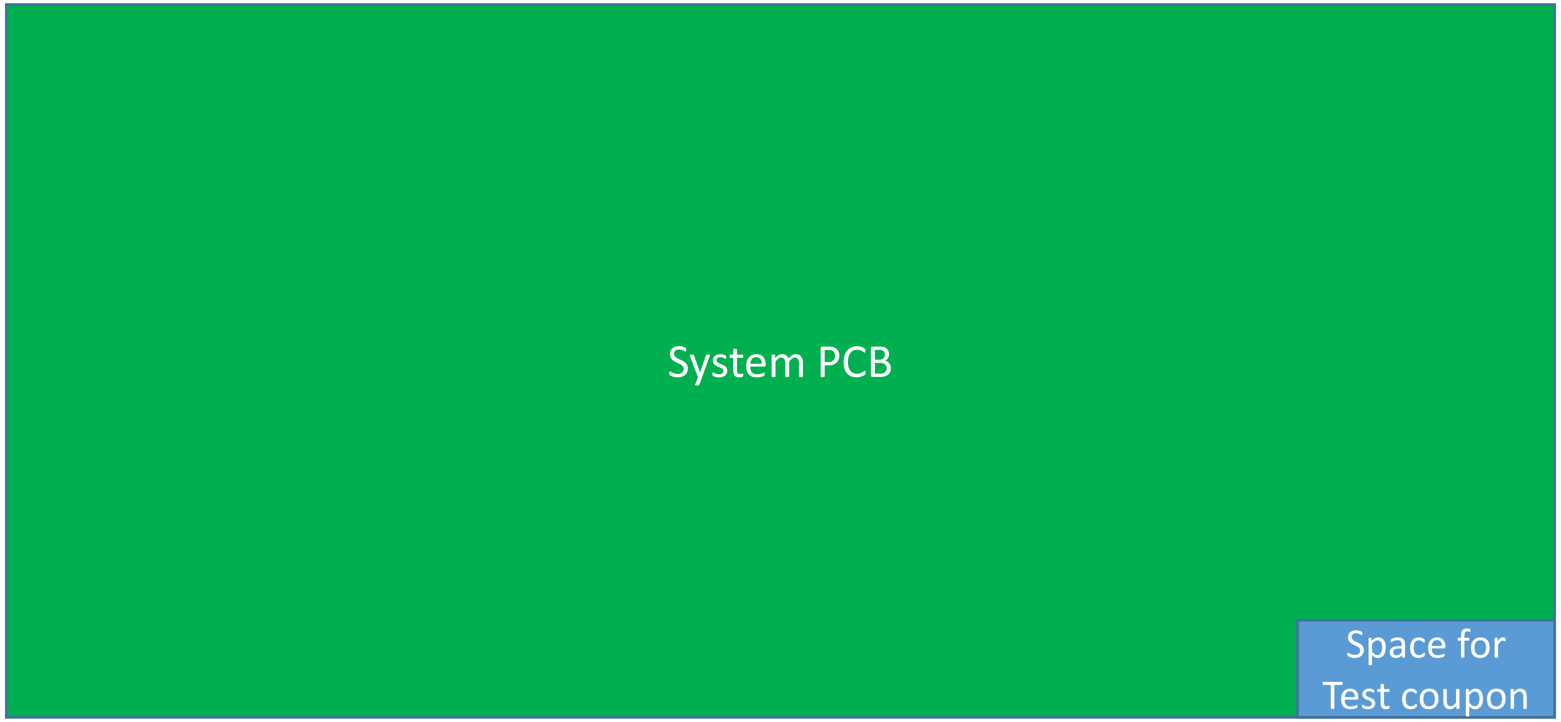
DesignCon 2019
WHERE THE CHIP MEETS THE BOARD

Probe study conclusion

- De-embedded IL, RL and TDR results are very close to 2.92mm results.
- With measured dimensions taken into account (dielectric thickness, trace width, Rq), all extracted parameters show little difference, within 5%.

Limited space conditions

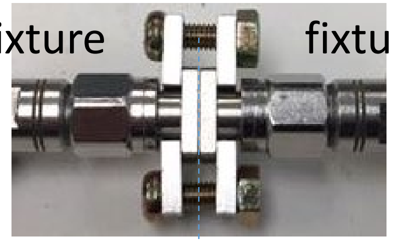
- What if you wanted to characterize the material of a board you designed, but there is only enough space on your board to include a single line for a test coupon?
- Will you be able to characterize the material without a 2x thru for de-embedding?



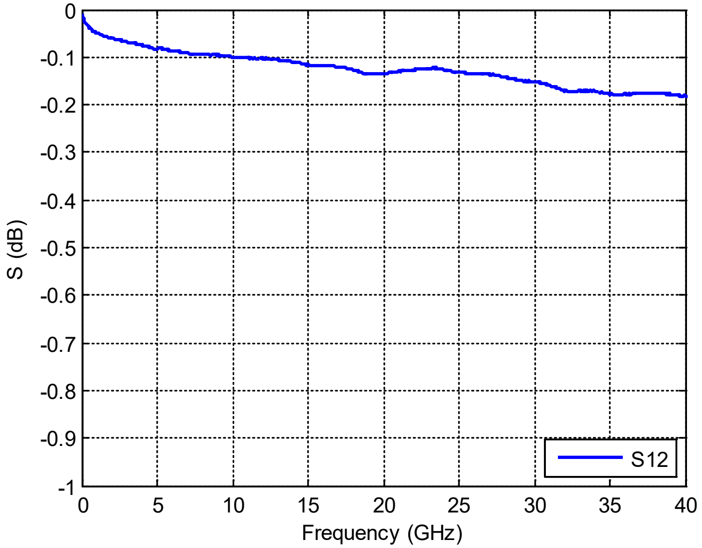
Fixture-fixture measurements

- The back-to-back connectors' insertion loss and return loss do not cross within the 40GHz range, which meets the criteria for de-embedding.

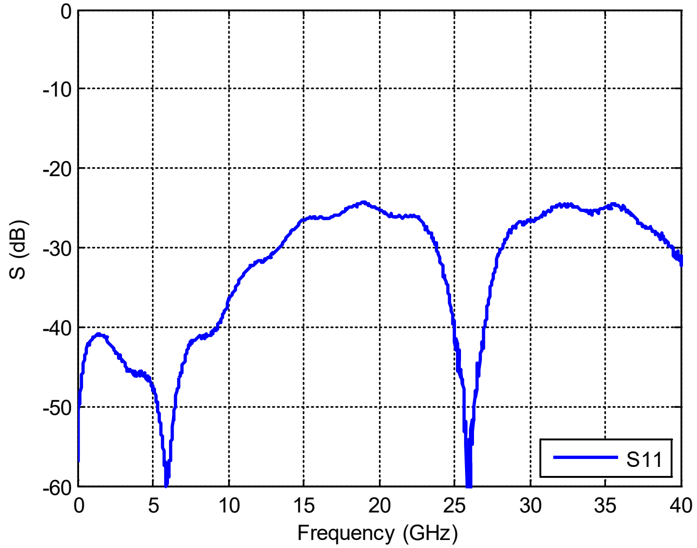
fixture fixture



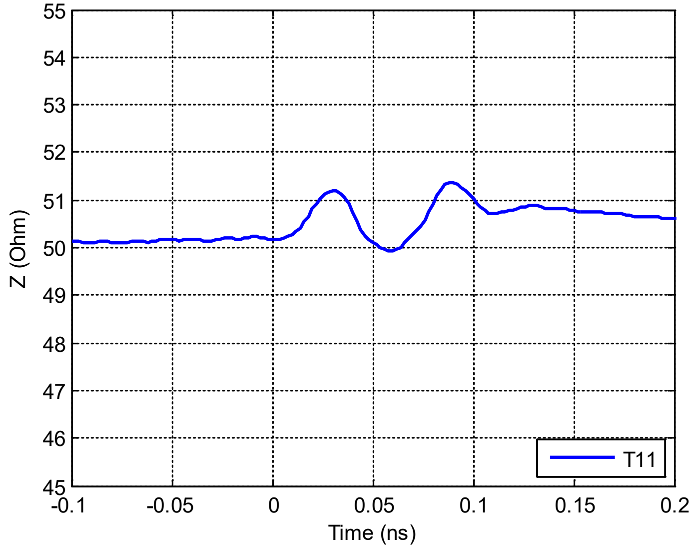
Insertion loss



Return loss



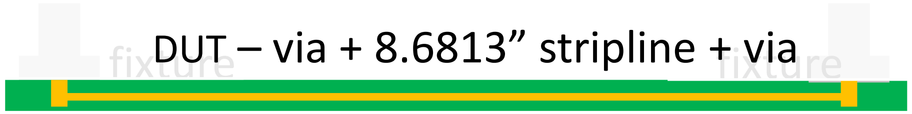
TDR @15ps Trise (20-80)



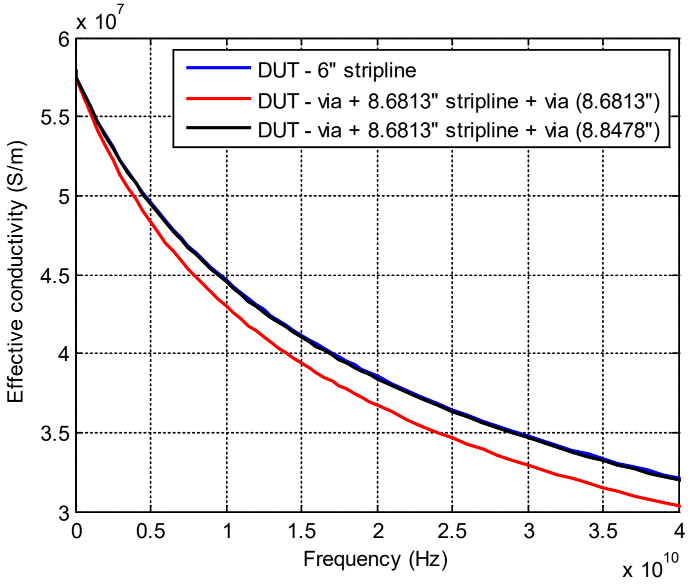
DesignCon 2019 WHERE THE CHIP MEETS THE BOARD

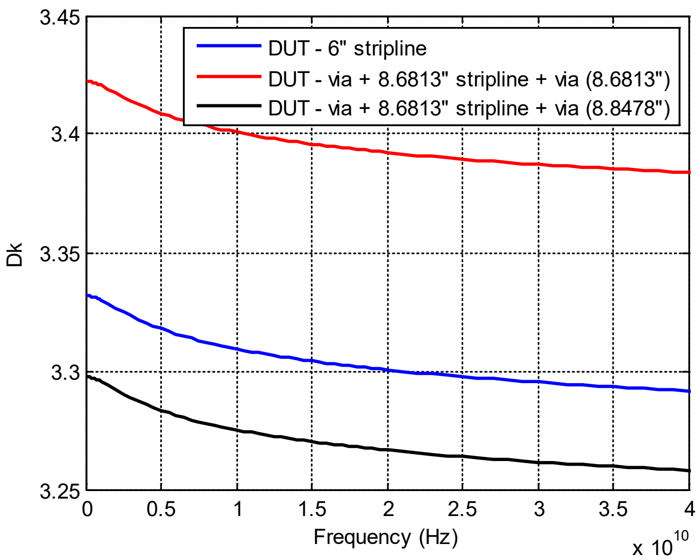
MPX extraction trace + via length

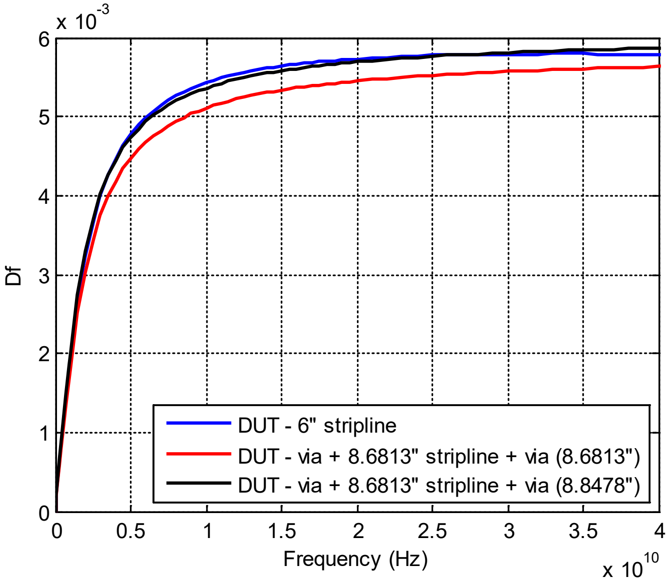
- Via length must be taken into account when extracting material properties.
- With backdrilled vias, fixture-less de-embedding can match the fixtured de-embedding results to about 2%.



vs.





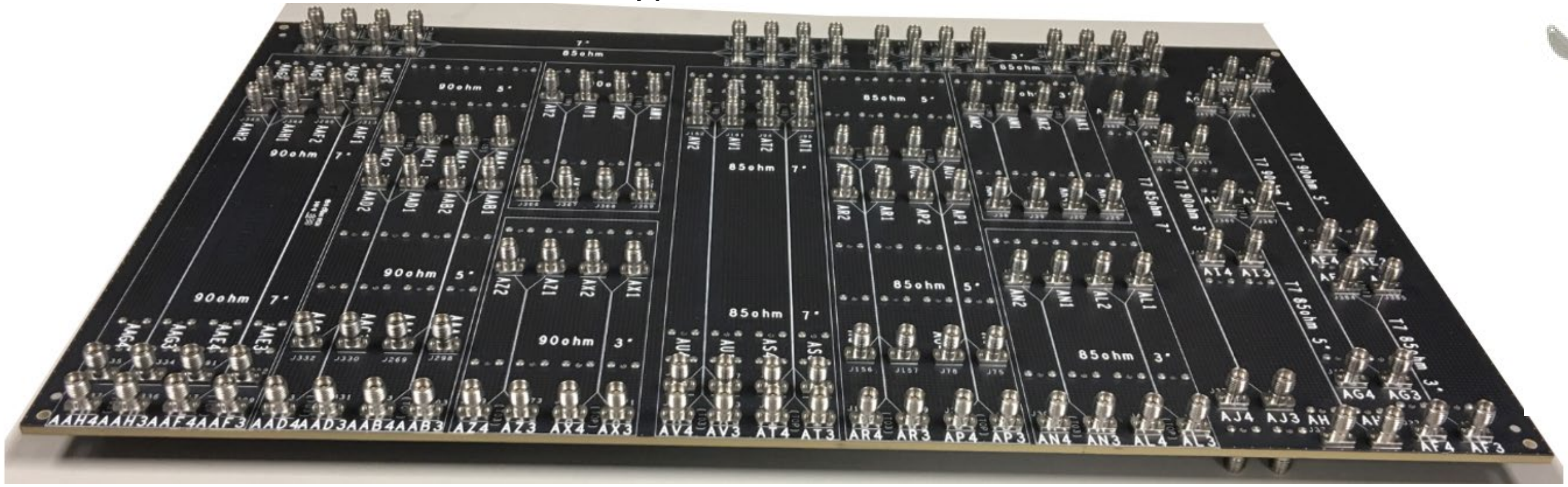


Test fixture design summary

- Test fixtures proposed in this MPX methodology is very simple and straight forward.
- The 2x thru has two requirements:
  - IL should not cross RL up to frequency of interest
  - IL should be resonance free up to frequency of interest
- Connectors, footprints, vias, and PCB trace lengths need to be carefully selected and designed in order to meet the above criteria.

SMA Challenge

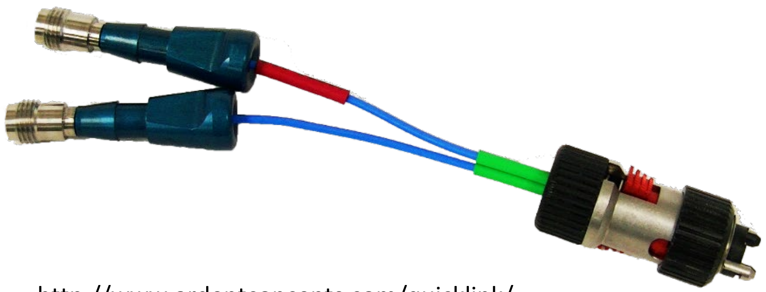
Typical SI test Board



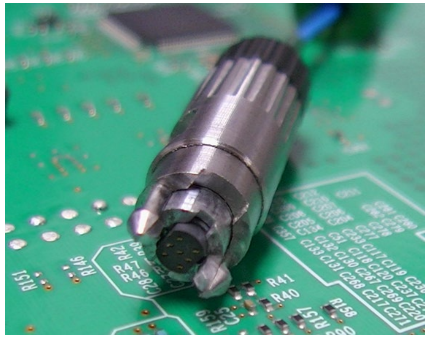
- SMA connectors are very reliable and robust → consistent results
- 100s of SMA connectors per board for detailed characterization across layers
- SMA assembly is manual → time consuming and labor intensive
- SMA cable attachment (requires Torque wrench) → time consuming & labor intensive
- SMA connectors occupy considerable area on the board
- ***Need alternate connector solution for rapid measurements with smaller connector foot print***

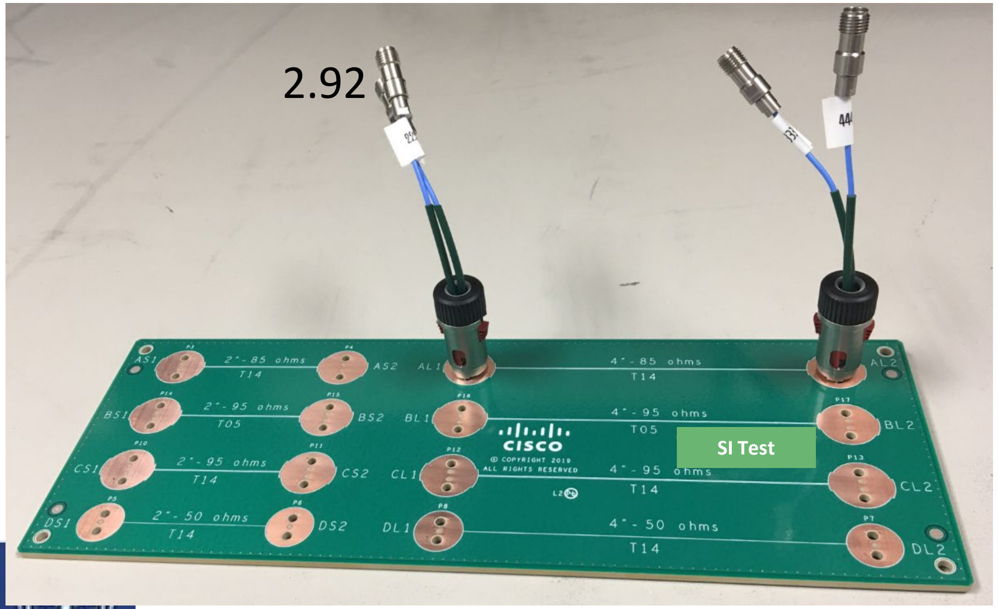
Quicklink Connectors Enable Rapid Measurements

1.85



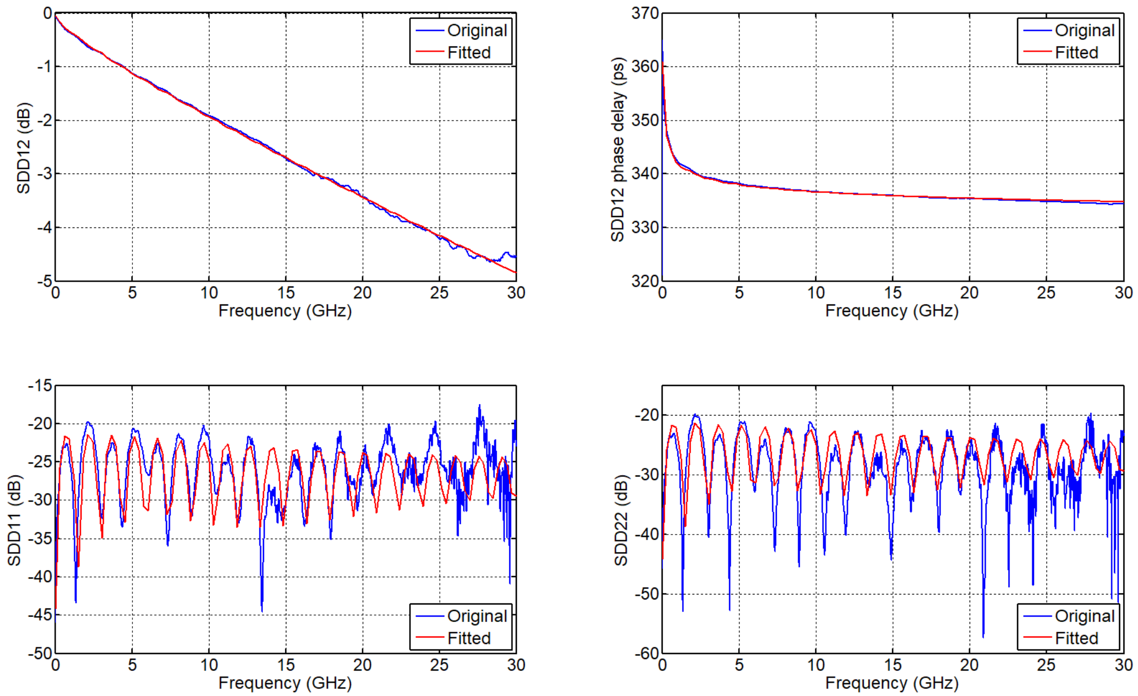
http://www.ardentconcepts.com/quicklink/





- Push & Twist mechanism → less effort for assembly & removal
- No need to remove VNA cables once attached
- Only two connectors required for entire board
- High Bandwidth response
- Well suited for PCB characterization in lab & production environments

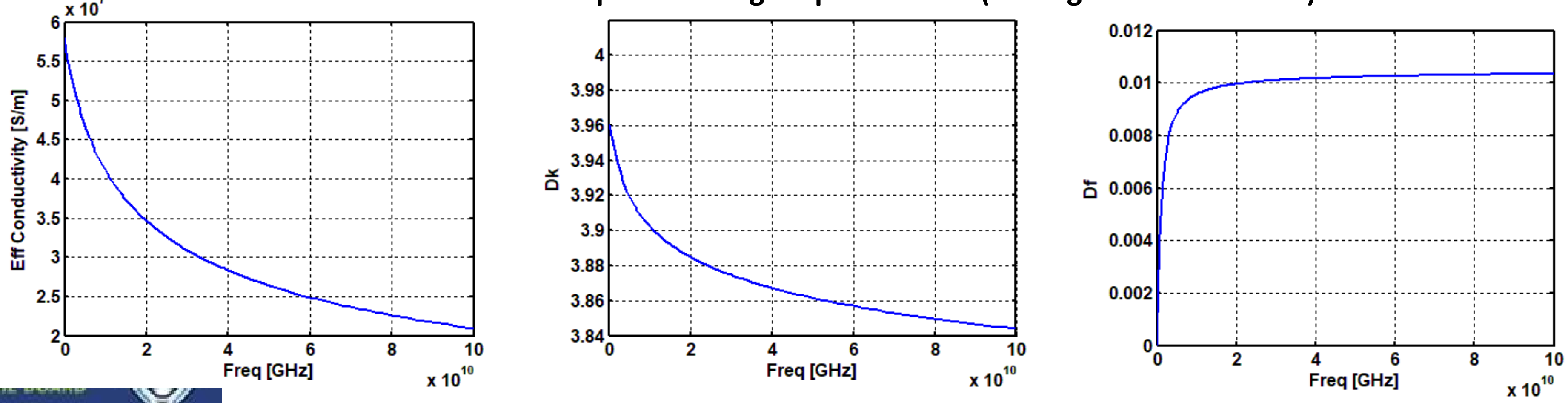
PCB Characterization with Quicklink : Results



- Quicklink Cable & Connector response deembedded
- Deembedded Tline matches well with Model

Thanks to Gert Hogenwarter, Gatewave Northern inc for Quicklink PCB footprint optimizations

Extracted Material Properties using stripline Model (homogeneous dielectric)

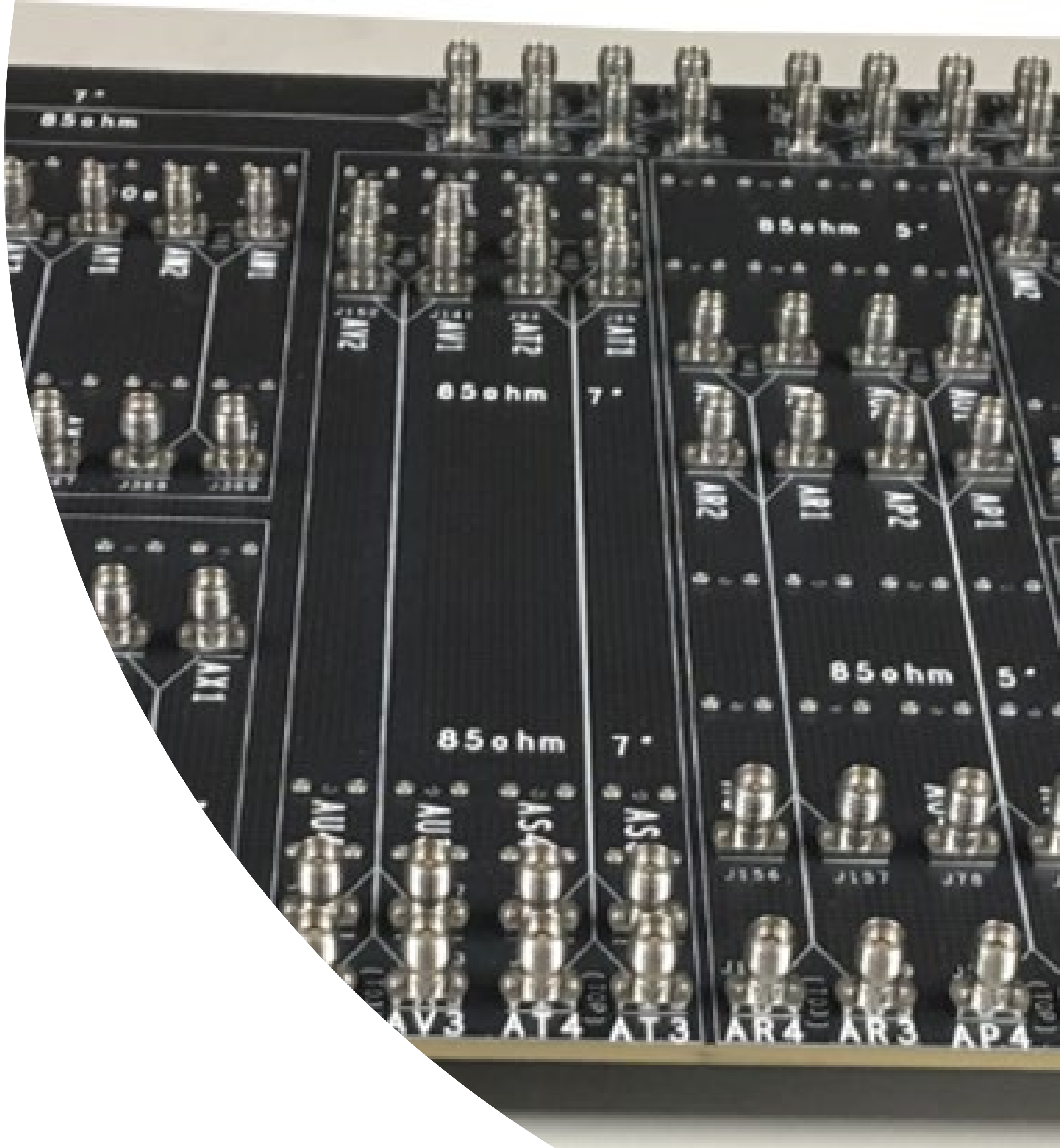


Outline

- Introduction : J. Balachandran - Cisco inc
- PCB Material Characterization Theory : Ching Chao - Ataitec Corp
- Modeling PCB Interconnects : Alvin - Hirose Electricals
- Addressing Skew impairments : Clement Luk, Samtec
- Test Fixture Design : Jeremy Baun - Hirose Electricals, J. Balachandran
- Automation : J. Balachandran
- Case Study & Results : Anna Gao – Cisco inc
- Summary : Ching Chao

PCB material characterization is challenging

- 100s of s-param files
  - Multiple layers
  - Different impedances (85, 90, 100 Ω etc)
  - Several dielectric material choices (Standard loss, Mid loss, low loss etc)
  - Varying Cu thickness and surface roughness (HVLP, VLP, RTF etc)
  - Different types of Fiber weaves (2110, 3116 etc) , resin contents
  - Multiple Fab Vendors
- PCB Material Characterization is a big data problem



Characterizing PCB channels

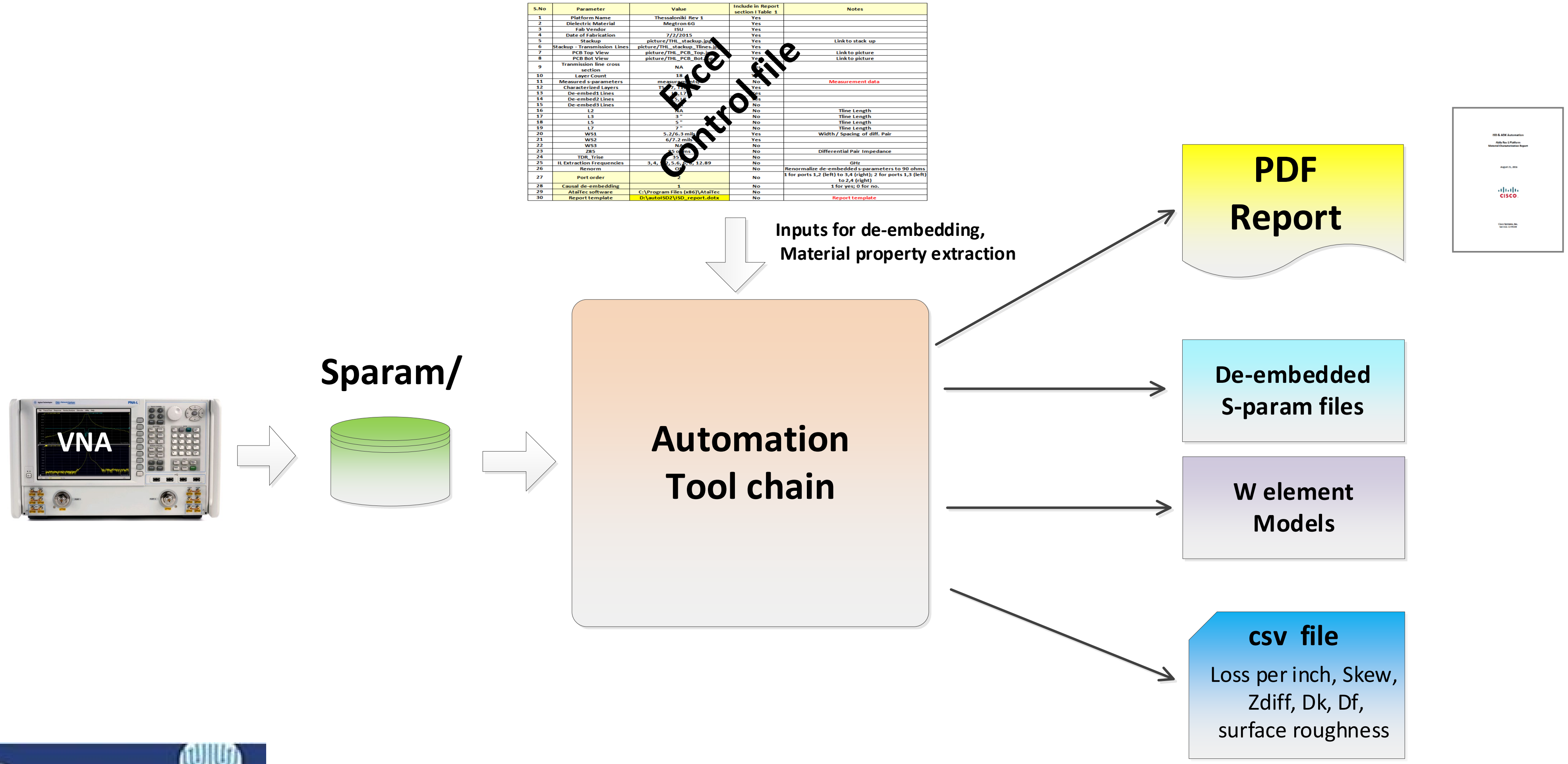
Key parameters of interest

- Insertion loss per inch
- Differential Impedance
- Diff. Pair Skew
- DK, DF
- Cu Surface roughness

Qualitative Analysis (Insertion loss per inch, Differential Impedance, Diff. Pair Skew)

Electrical Models (DK, DF, Cu Surface roughness)

Automation Framework



Excel Control File that Enables Automation – Example

S.No	Parameter	Value	Include in Report	Notes
1	Platform Name	Abila	Yes	
2	Dielectric Material	Megtron 6G	Yes	
3	Fab Vendor	xxxx	Yes	
4	Date of Fabrication	1/11/2018	Yes	
5	Stackup	picture/THL_stackup.jpg	Yes	Link to stack up
6	Stackup - Transmission Lines	picture/THL_stackup_Tlines.jpg	Yes	
7	PCB Top View	picture/THL_PCB_Top.jpg	Yes	Link to picture
8	PCB Bot View	picture/THL_PCB_Bot.jpg	Yes	Link to picture
9	Tranmission line cross section	NA	No	
10	Layer Count	18	Yes	
11	Measured s-parameters	measurements/	No	Measurement data
12	Characterized Layers	T5, T7, T12, T14	Yes	
13	De-embed1 Lines	L3, L7	Yes	
14	De-embed2 Lines	L5, L7	Yes	
15	De-embed3 Lines	NA	No	
16	L2	NA	No	Tline Length
17	L3	3 "	No	Tline Length
18	L5	5 "	No	Tline Length
19	L7	7 "	No	Tline Length
20	WS1	5.2/6.3 mils	Yes	Width / Spacing of diff. Pair
21	WS2	6/7.2 mils	Yes	
22	WS3	NA	No	
23	Z85	85 ohms	No	Differential Pair Impedance
24	TDR_Trise	12.5 ps	No	
25	IL Extraction Frequencies	3, 4, 5.2, 5.6, 6, 8, 12.89, 14, 28	No	GHz
26	Renorm	ON	No	Renormalize de-embedded s-parameters to 85 ohms
27	Port order	2	No	1 for ports 1,2 (left) to 3,4 (right); 2 for ports 1,3 (left) to 2,4 (right)
28	Causal de-embedding	1	No	1 for yes; 0 for no.
29	AtaiTec software	C:\Program Files (x86)\AtaiTec	No	
30	Report template	D:\autoISD2\ISD_report.dotx	No	Report template

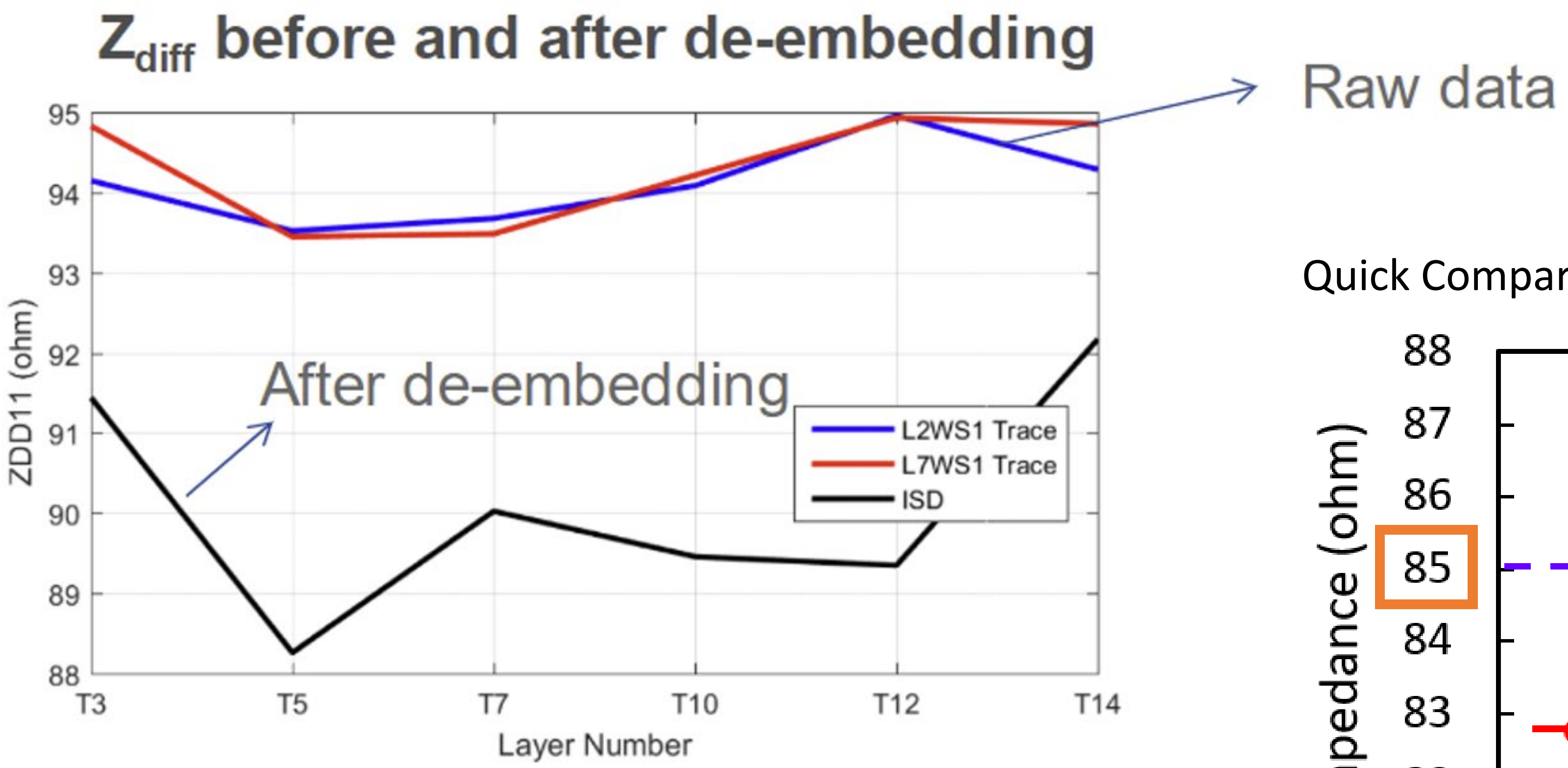
Insertion Loss Example

Insertion Loss [dB / inch]

Freq	Layer 3	Layer 5	Layer 7	Layer 10	Layer 12	Layer 14
GHz	L2L7T3WS1	L2L7T5WS1	L2L7T7WS1	L2L7T10WS1	L2L7T12WS1	L2L7T14WS1
3	-0.200208	-0.214174	-0.23112	-0.230748	-0.210656	-0.198021
4	-0.240618	-0.257358	-0.279482	-0.277466	-0.253062	-0.237836
5.2	-0.290562	-0.309116	-0.334012	-0.337278	-0.304094	-0.285004
5.6	-0.307278	-0.326626	-0.352522	-0.358242	-0.32128	-0.303108
6	-0.324214	-0.345294	-0.371136	-0.37261	-0.33808	-0.32046
8	-0.403222	-0.426578	-0.459442	-0.457102	-0.419742	-0.393126
12.89	-0.59184	-0.623564	-0.67018	-0.665518	-0.612678	-0.573016

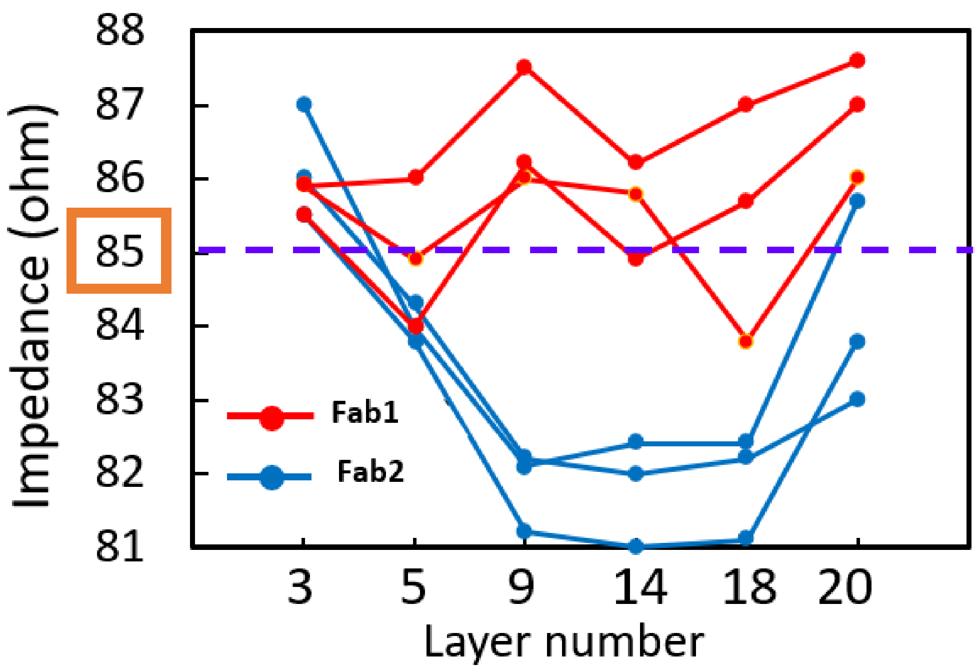
17 % difference in IL across layers

Diff. Impedance Example



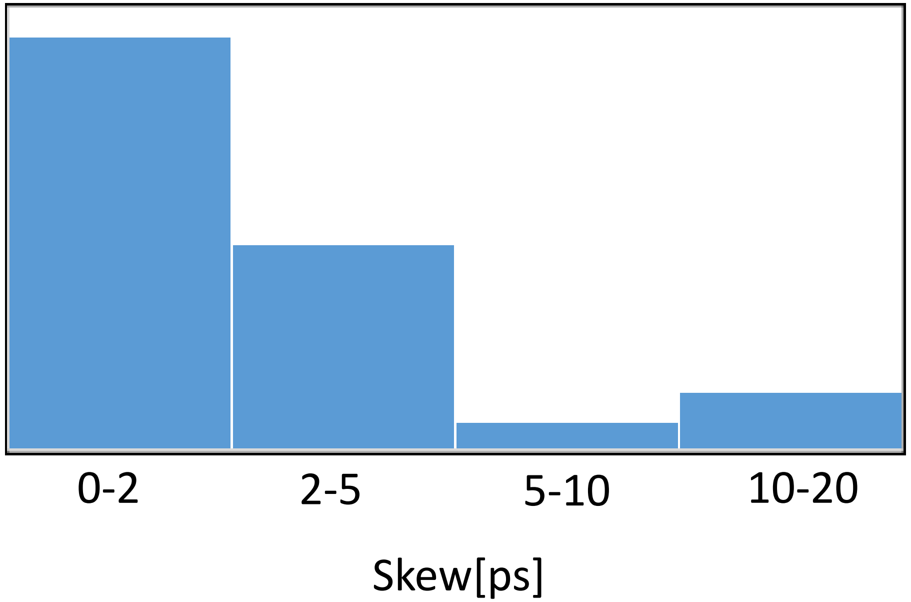
Quick Comparison of impedance control across layers

Quick Comparison of impedance control between fabs



Diff Pair Skew Example

Skew histogram plot taken from all Diff. Pair measurements in the SI Test board



Automation Summary

- PCB Material Characterization is a big data problem
- Automation is essential
- Discussed methodology for Automation & provided examples

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Case study & results

Outline

- Background Information
- T-line modeling for material characterization
  - Homogeneous vs inhomogeneous stripline models
- Impact of SR on DF extraction
- Skew impact on insertion loss and material characterization
- Temperature Impact on material characterization
- Summary

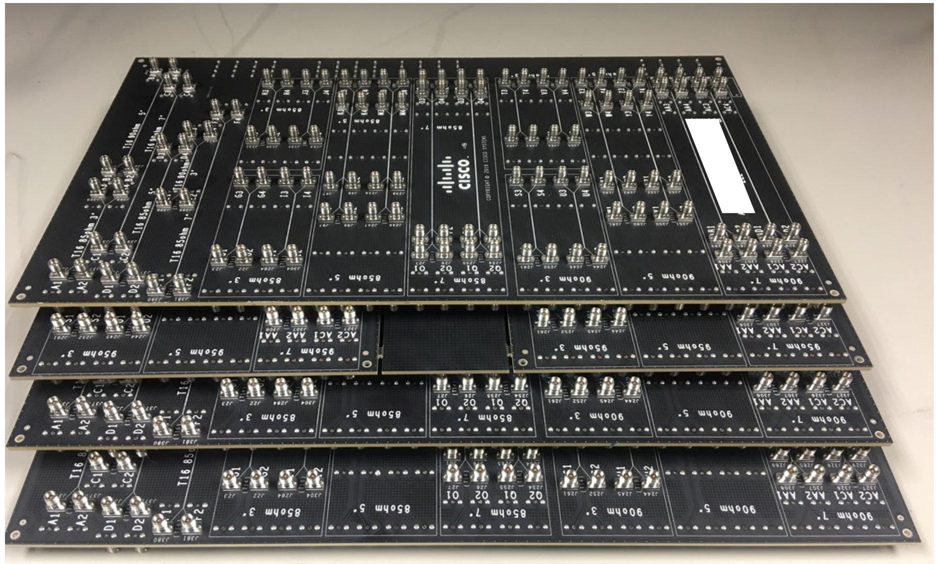
Background information on material characterization case study

VNA measurements of Long & short traces → **2X thru de-embedding** → De-embedded .s4p → **Tline Model Fit** → DK, DF vs freq; W & WO SR **<u>Homogeous/ Inhomogenous model</u>** → Fitted .s4p (Correlated with VNA measurements)

MPX Methodology

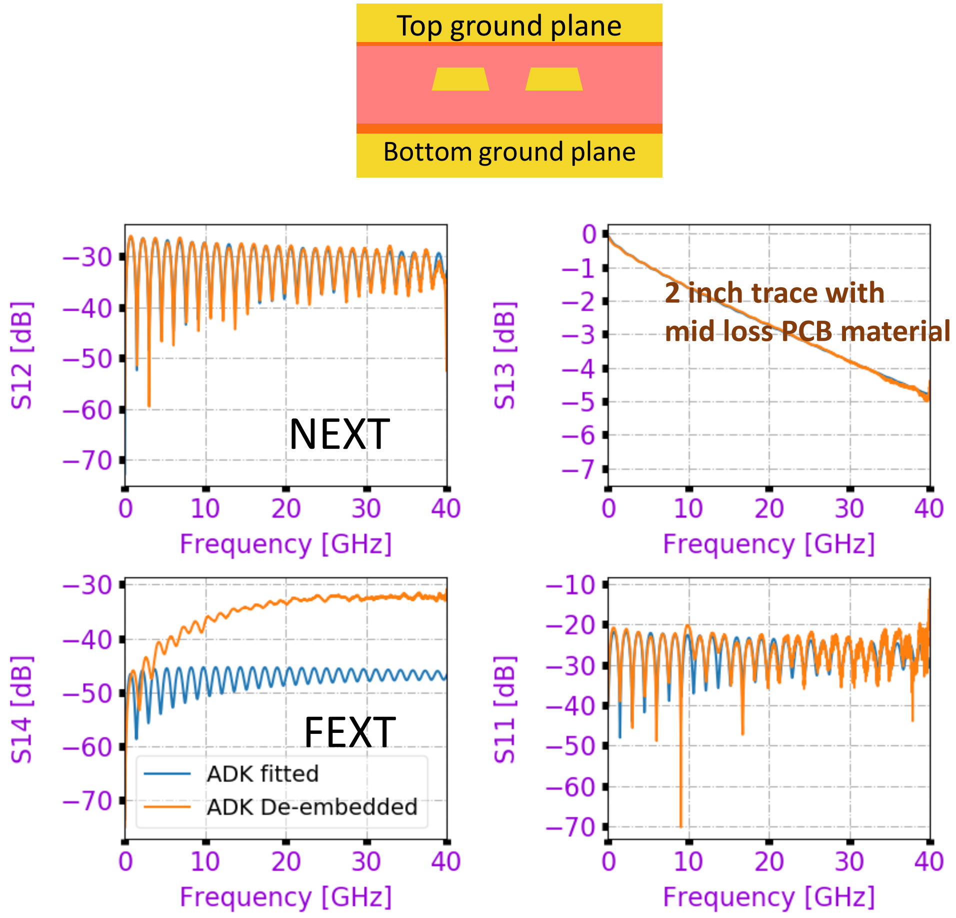
- A good correlation between de-embedded and fitted data proves the accuracy of Dk & DF extraction.

- VNA measurements performed on multiple boards with high/mid/low loss materials

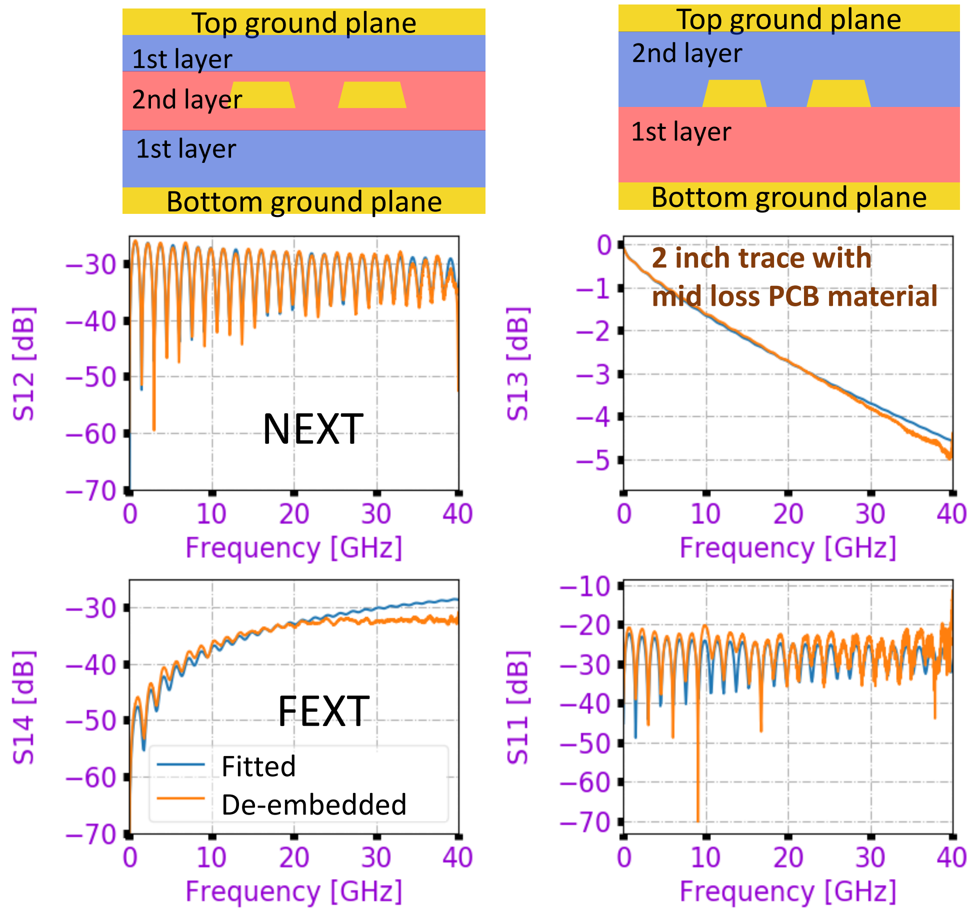


Homogeneous vs inhomogeneous models for T-line modeling

Homogeneous Model



Inhomogeneous Model (For 2-layer and 3-layer model)



- Both homogeneous and inhomogeneous models correlate well with measurements
- Homogeneous model sufficient for IL / RL modeling
- For accurate FEXT, inhomogeneous model required

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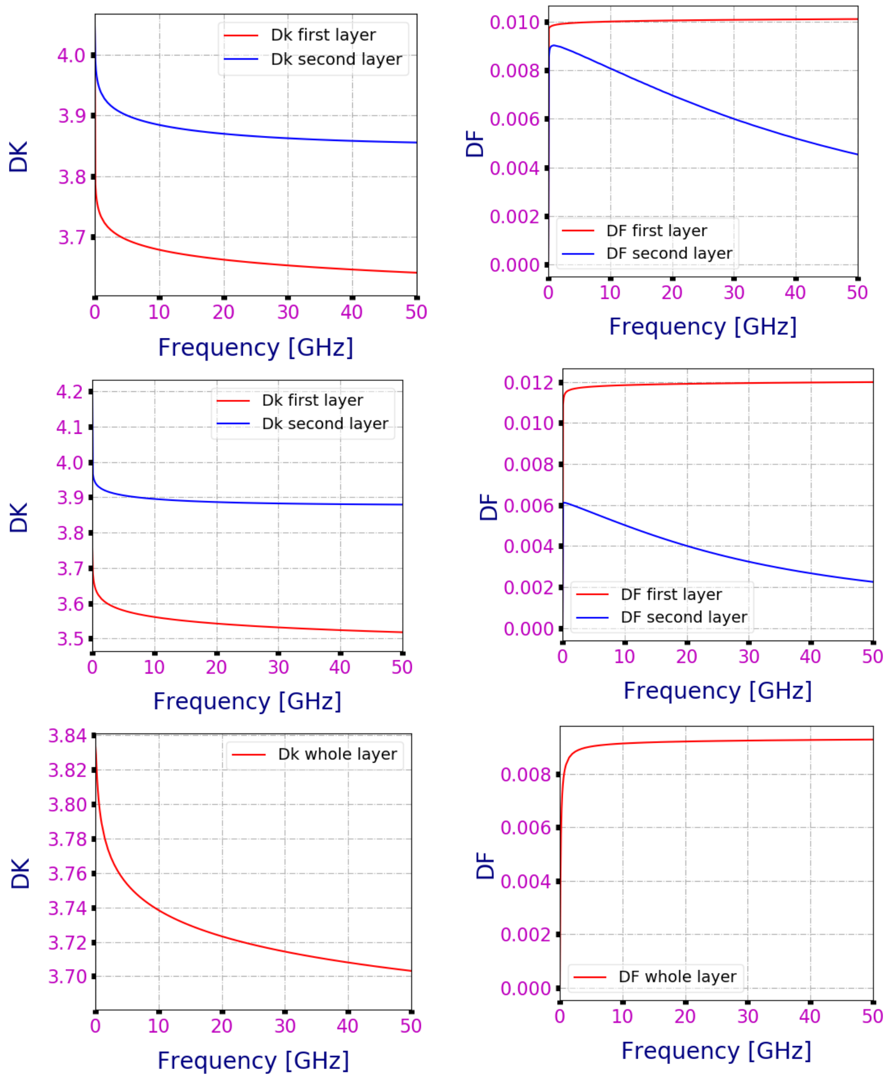
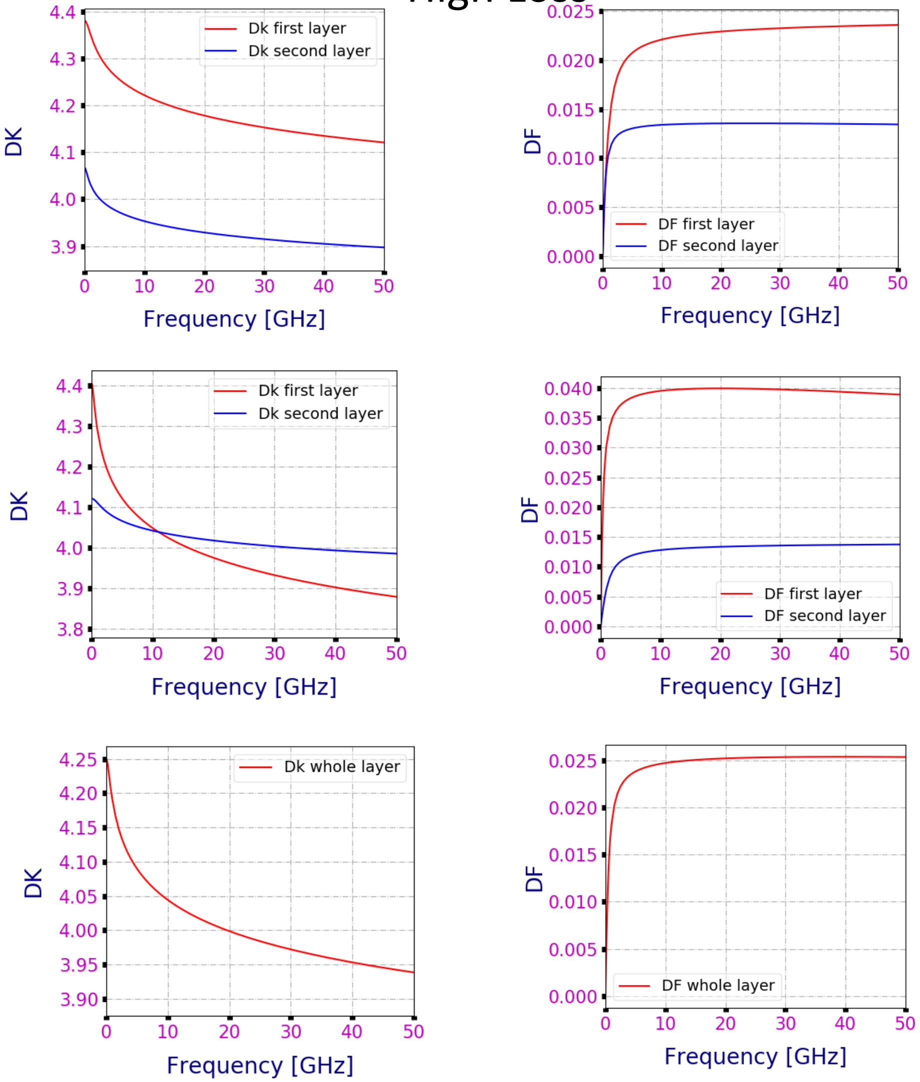
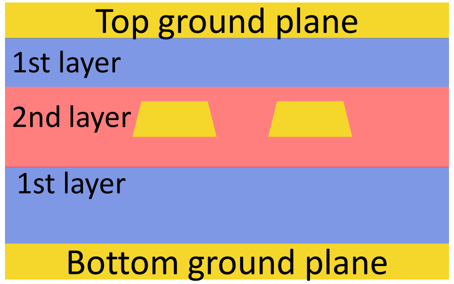
DK & DF extraction using homogeneous and inhomogeneous models

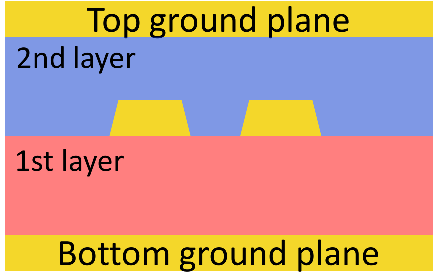
Mid Loss

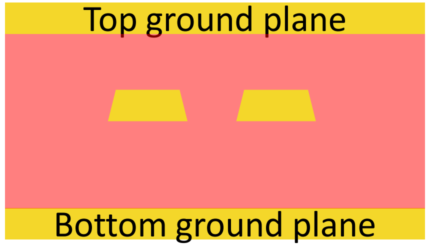


High Loss



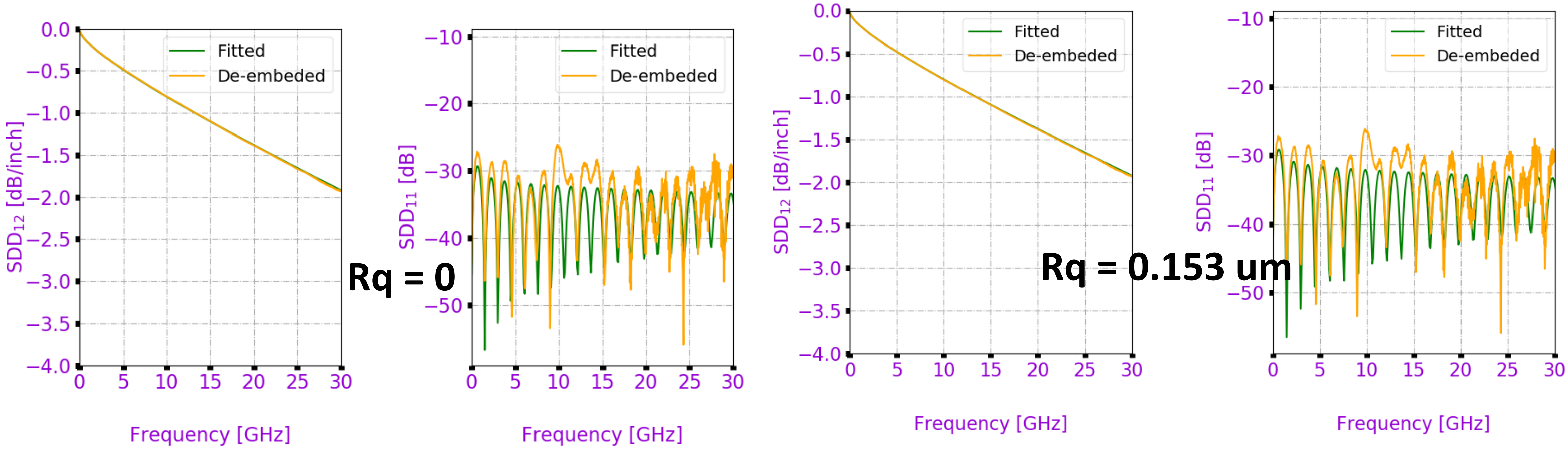






- Mid loss material has different DF distribution compared to low loss material

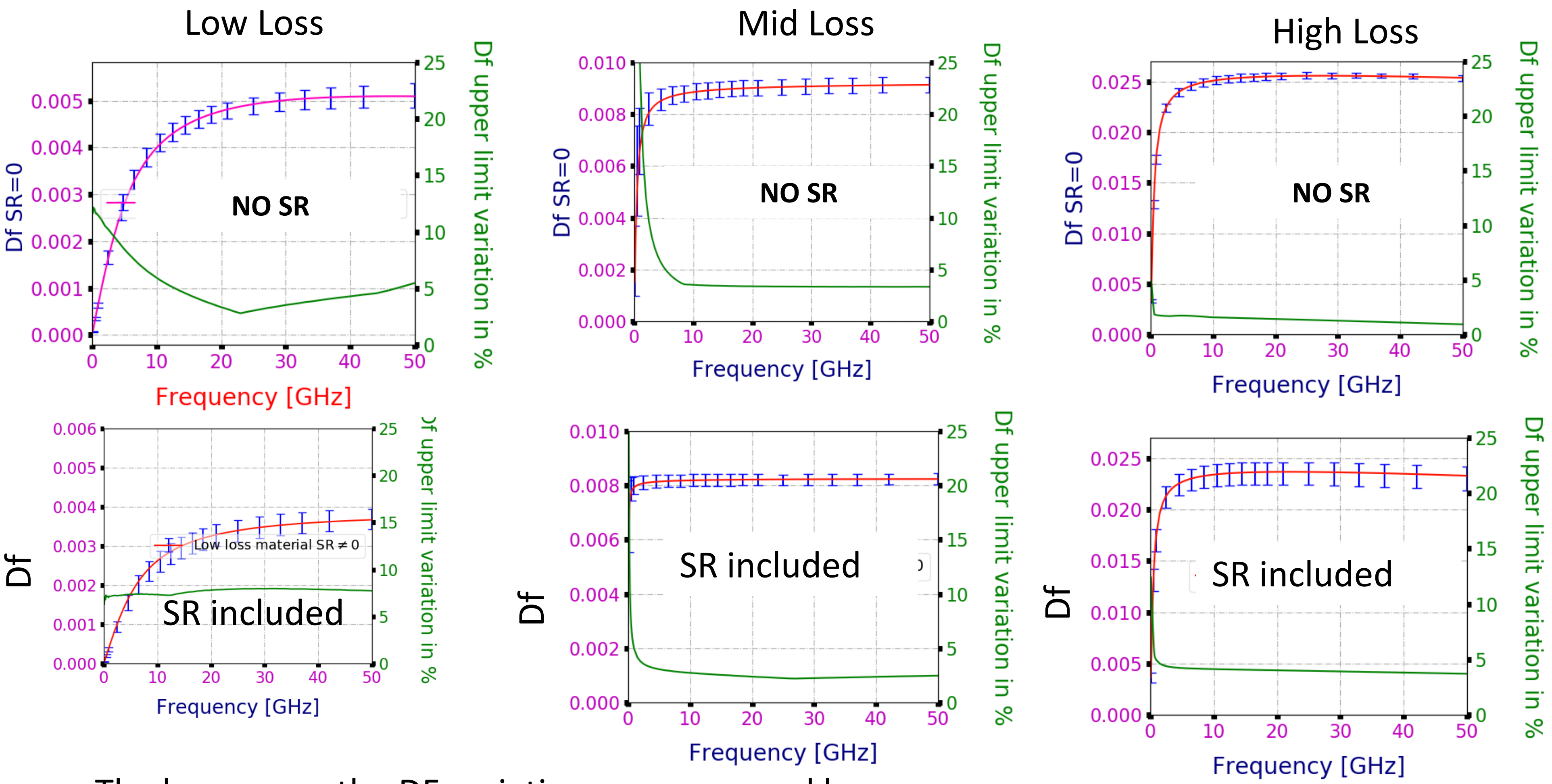
Loss due to surface roughness can be lumped into dielectric loss for model simplicity

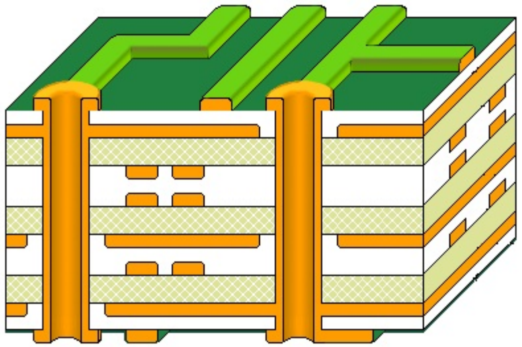


- Different tools have difference SR model. To simplified the process, we combine the surface roughness into DF

- Good fit can be obtained with or without SR

Dielectric loss with / without considering Surface Roughness (SR) across layers

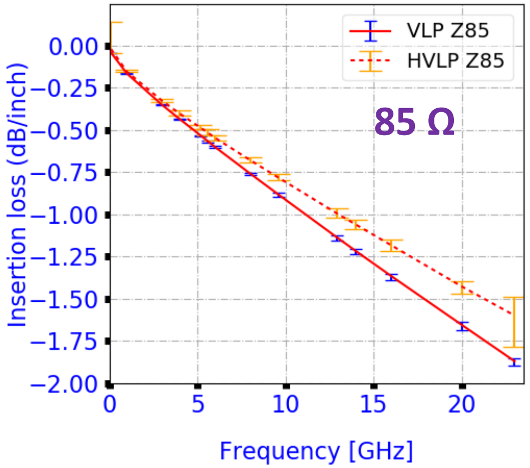


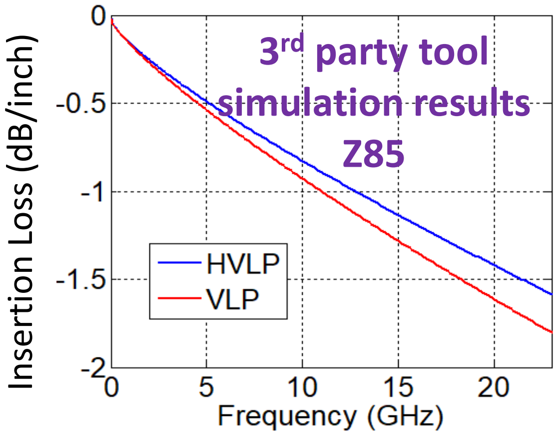


- The bar means the DF variation across several layers
- High loss material has lower DF variation across layers than low loss material

Comparison of insertion loss for HVLP and VLP

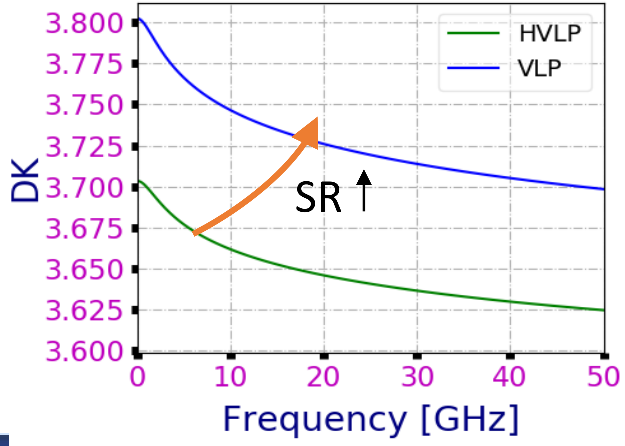
- The measured traces with the same impedance have the same geometry design, dielectric material (mid loss material) , thickness and are fabricated by the same vendor
- The IL data are obtained by averaging de-embedded results of traces across 5 different layers
- Surface roughness (SR) is forced to be 0 when extracting DF (combining SR effect into DF for simplifying the process)

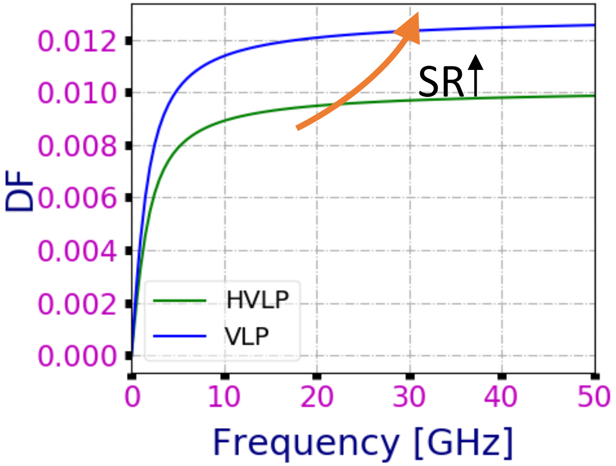




Conclusions:

- DK increases with surface roughness
- DF increases ~30 % for frequency > 5GHz

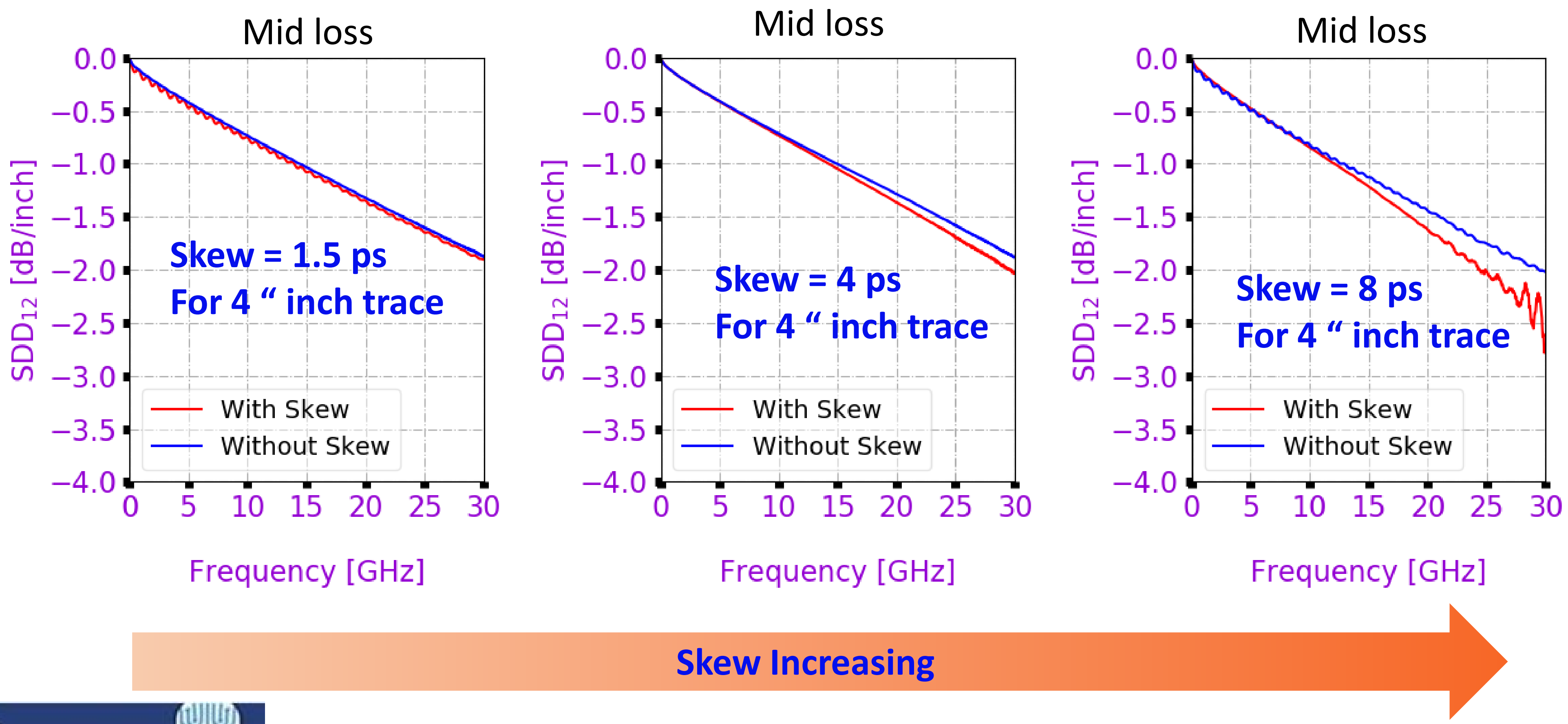




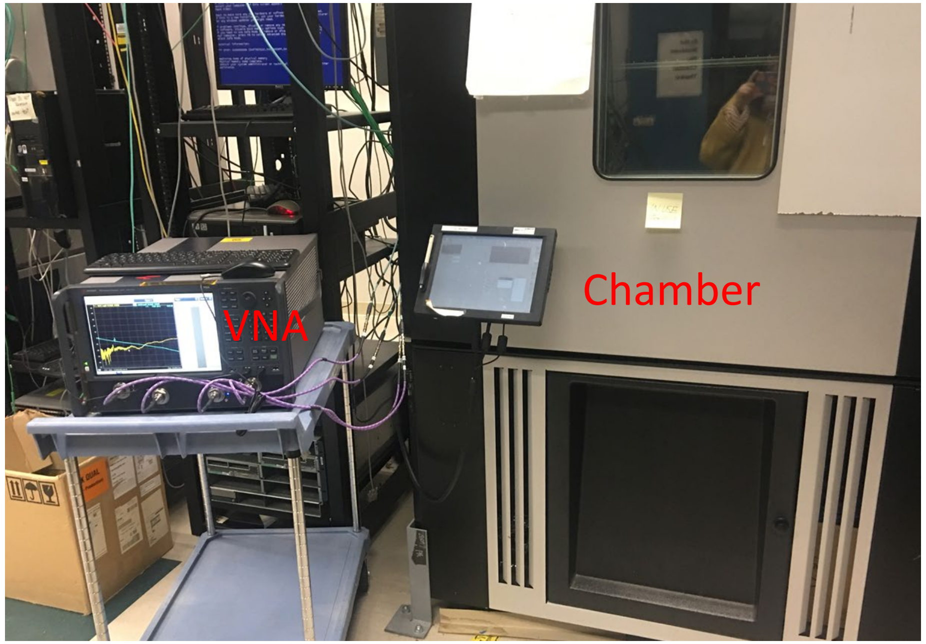
Comparison of de-embedded results without and with skew

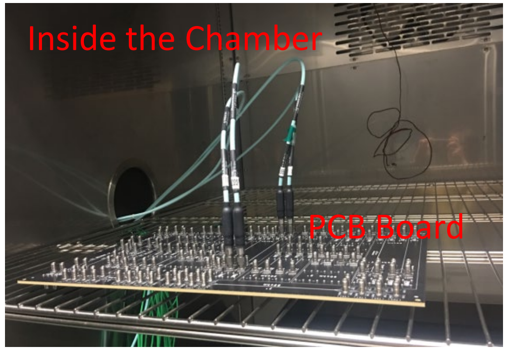
- The measurement data show that skew can affect the accuracy of the de-embedded process and thus MPX results
- The fiber-weave effect can add skew into s-parameter measurements

➢ Recommend to de-skew before DK and DF extraction



Temperature impact on the insertion loss

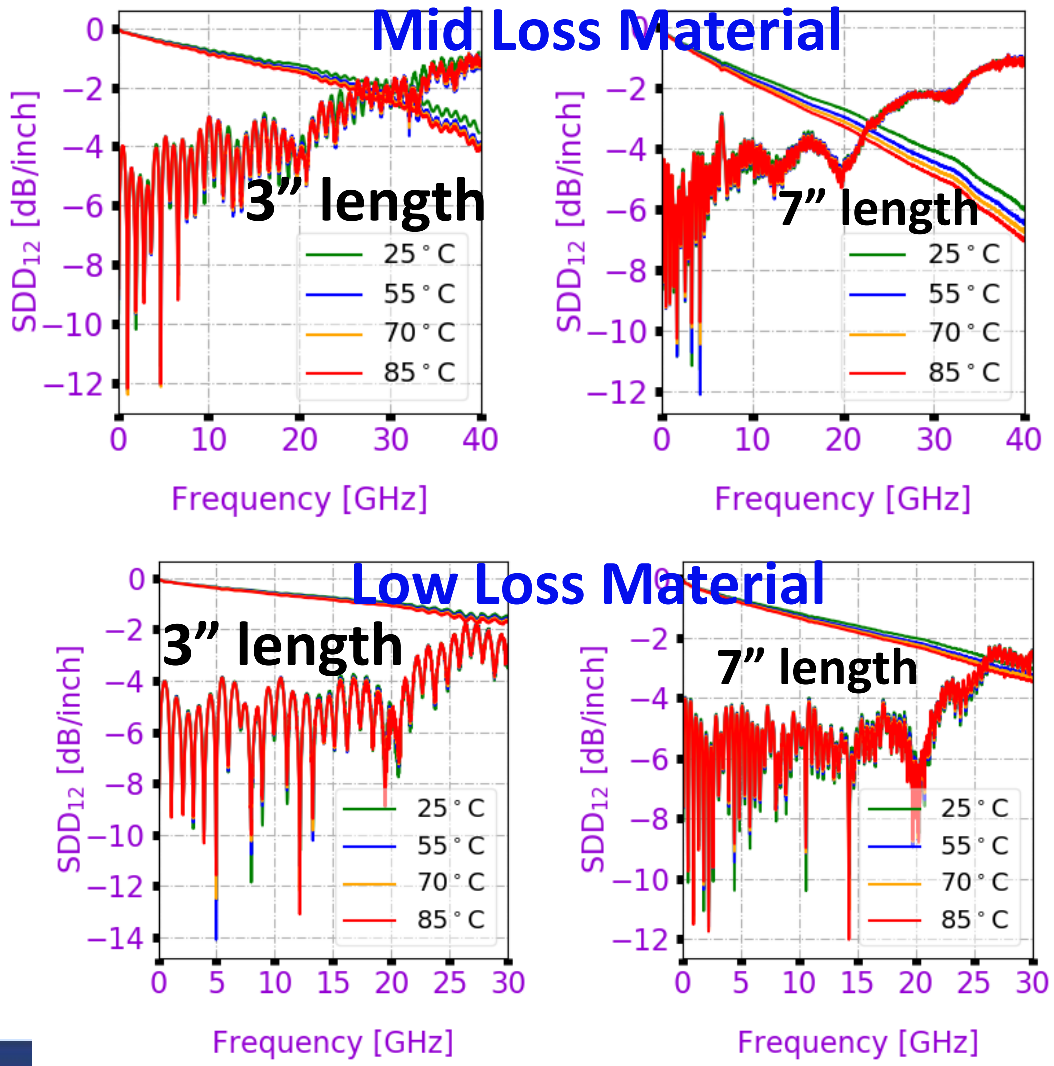




Calibration of VNA at room temperature → Put PCB board into chamber and increase the temperature to 55 º C with speed of 3 ºC/min → Hold the temperature at 55 º C for 1 hr and do the measurement → Increase the temperature to 70 º C with speed of 3 ºC/min, hold for 1 hr and do the measurement → Increase the temperature to 85 º C with speed of 3 ºC/min, hold for 1 hr and do the measurement → De-embedded the measurement data

- PCB board is held at the desired temperature for **1 hr** before VNA measurement
- VNA calibrated at room temperature
- Cable length inside the chamber should be as short as possible. Long cable (25 inch) will add **~2 % extra loss** to the final results compared to the short cable.

S-parameter measurement at different temperatures

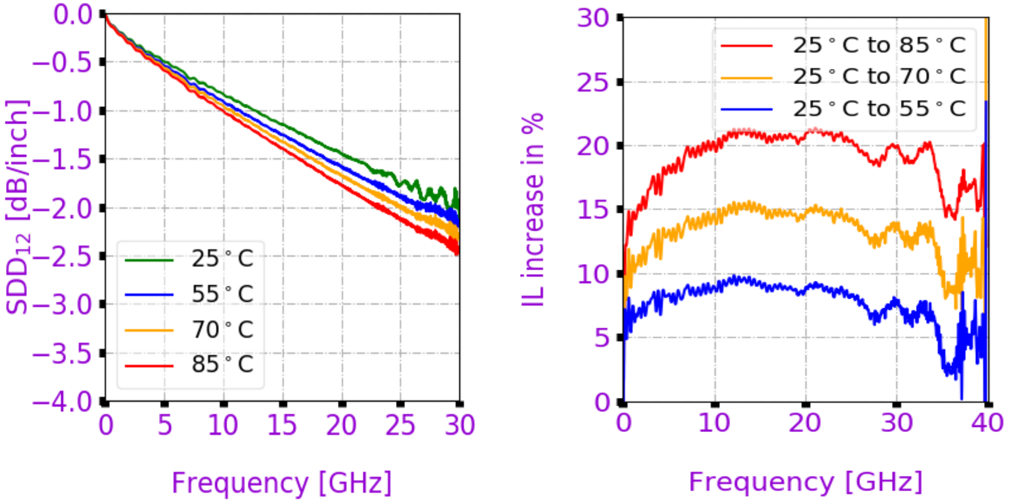


- Mid loss material and low loss material are studied
- Differential traces with 85 Ω

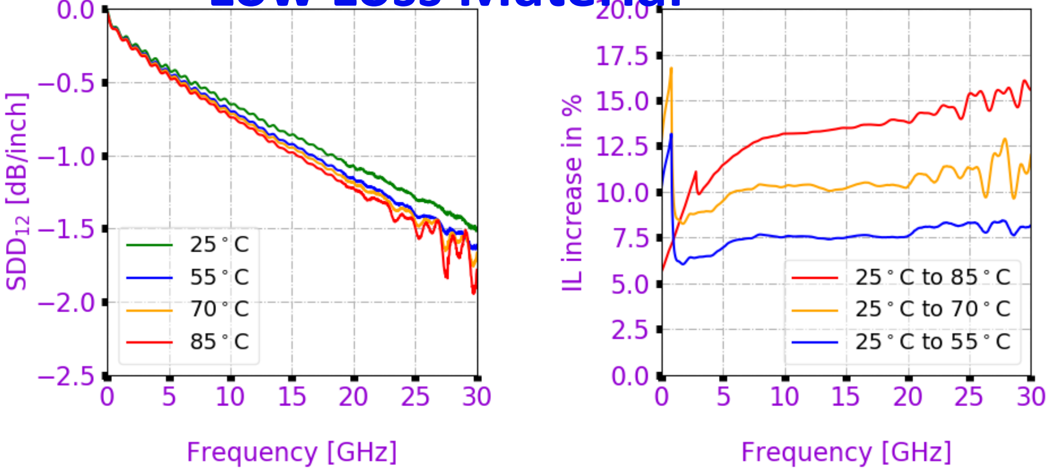
➢ Return loss is not affected by temperature

De-embedded insertion loss at different temperatures

Mid Loss Material



Low Loss Material



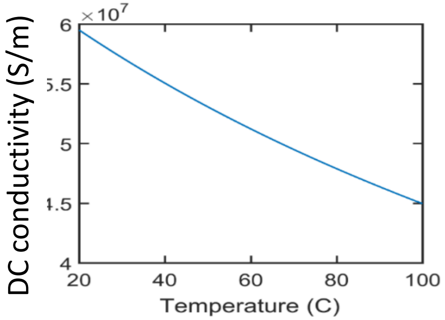
- 2X thru de-embedded method is used to minimize the effect of cable

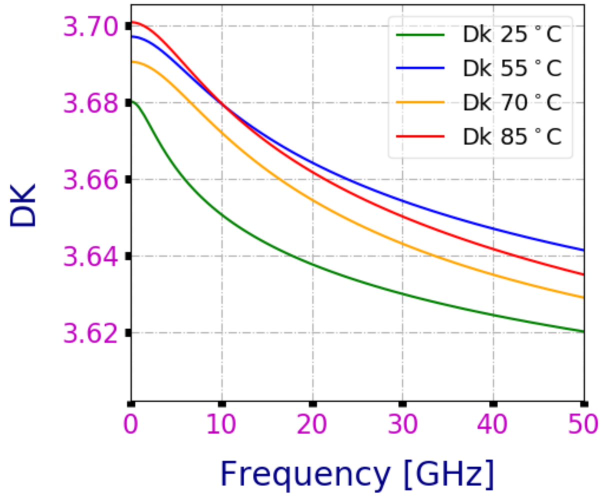
➢ Thermal Coefficient of Dissipation Factor (TCDF) like spec is needed for digital applications

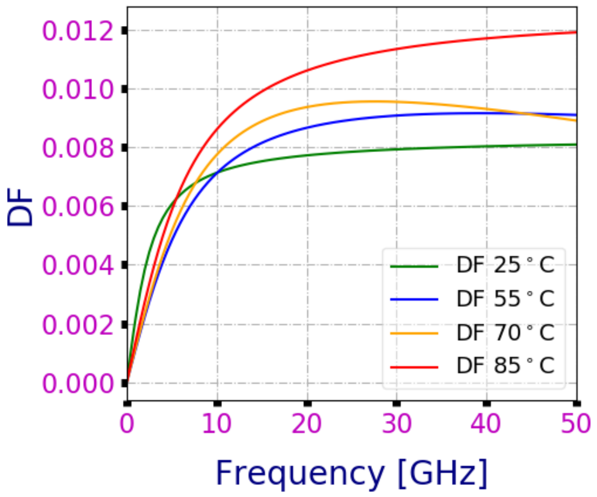
DK & DF extraction at different temperature

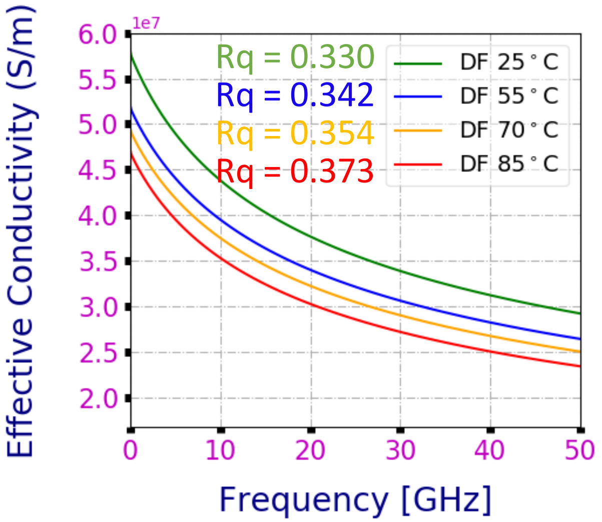
$$DC\ Conductivity\ (T) = \frac{1}{R(20°C) + R(20°C) \times (T - 20) \times \alpha}$$

$$\alpha = 0.00404; \quad R(20°C) = 1.68 \times 10^{-8}$$









- DC conductivity is a function of temperature
- Both conductor loss and dielectric loss increase as temperature rises
- Both DK and DF increases with temperature

Summary

- Characterized different PCB materials with std loss, mid loss and low loss characteristics
- Inhomogeneous model (2-layer and 3-layer) required for FEXT modeling
- Homogeneous model sufficient for insertion loss and return loss prediction
- Loss due to surface roughness can be lumped into dielectric loss for model simplicity
- The fiber-weave effect can impact insertion loss and thus dielectric modeling. Recommend de-skew before DKDF extraction
- Significant increase in Insertion loss at higher temperatures. Both conductor and dielectric loss increase with temperature

Outline

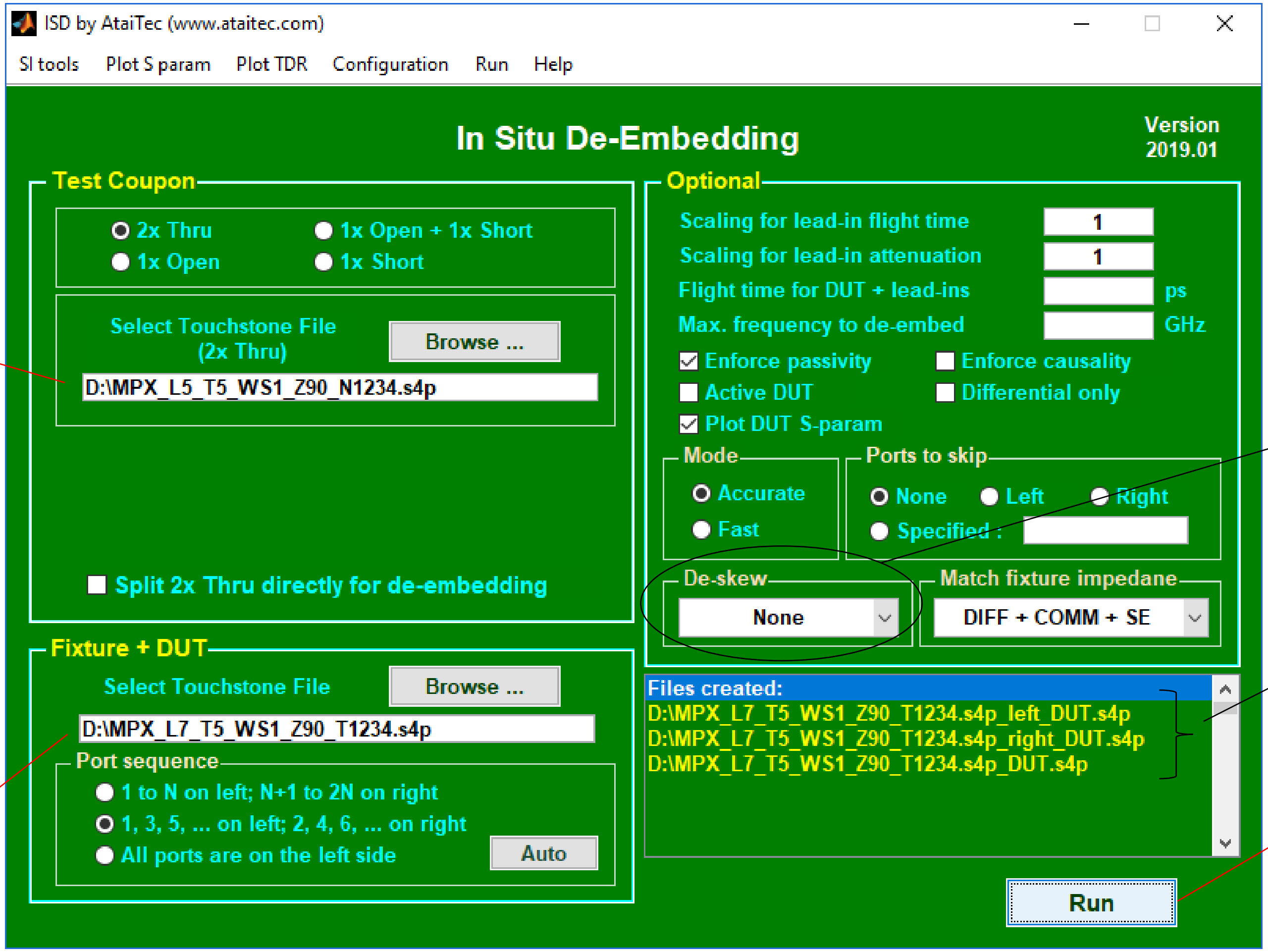
- Introduction : J. Balachandran - Cisco inc
- PCB Material Characterization Theory : Ching Chao Huang - Ataitec Corp
- Modeling PCB Interconnects : Alvin - Hirose Electricals
- Addressing Skew impairments : Clement Luk, Samtec
- Test Fixture Design : Jeremy Baun - Hirose Electricals, J. Balachandran
- Automation : J. Balachandran
- Case Study & Results : Anna Gao – Cisco inc
- Summary : Ching Chao Huang

Summary

Takeaways

- Self-consistent PCB material property extraction flow is presented.
  - Extracted models match all IL, RL, NEXT, FEXT and TDR/TDT.
- Djordjevic-Sarkar and Svensson-Dermer models are equivalent.
- Effective conductivity model can be curvefitted to Huray model.
- In-Situ De-embedding (ISD) addresses impedance variation by software, not hardware.
- Eigenvalue (Delta L) solution is prone to spikes.
- Many de-embedding and DK/DF/SR extraction examples are shown.
  - Connector vs. probe measurements
  - Various PCB materials
  - Skew and temperature effect
  - Effect of 2D models
- Automation

In-Situ De-embedding (ISD)



1

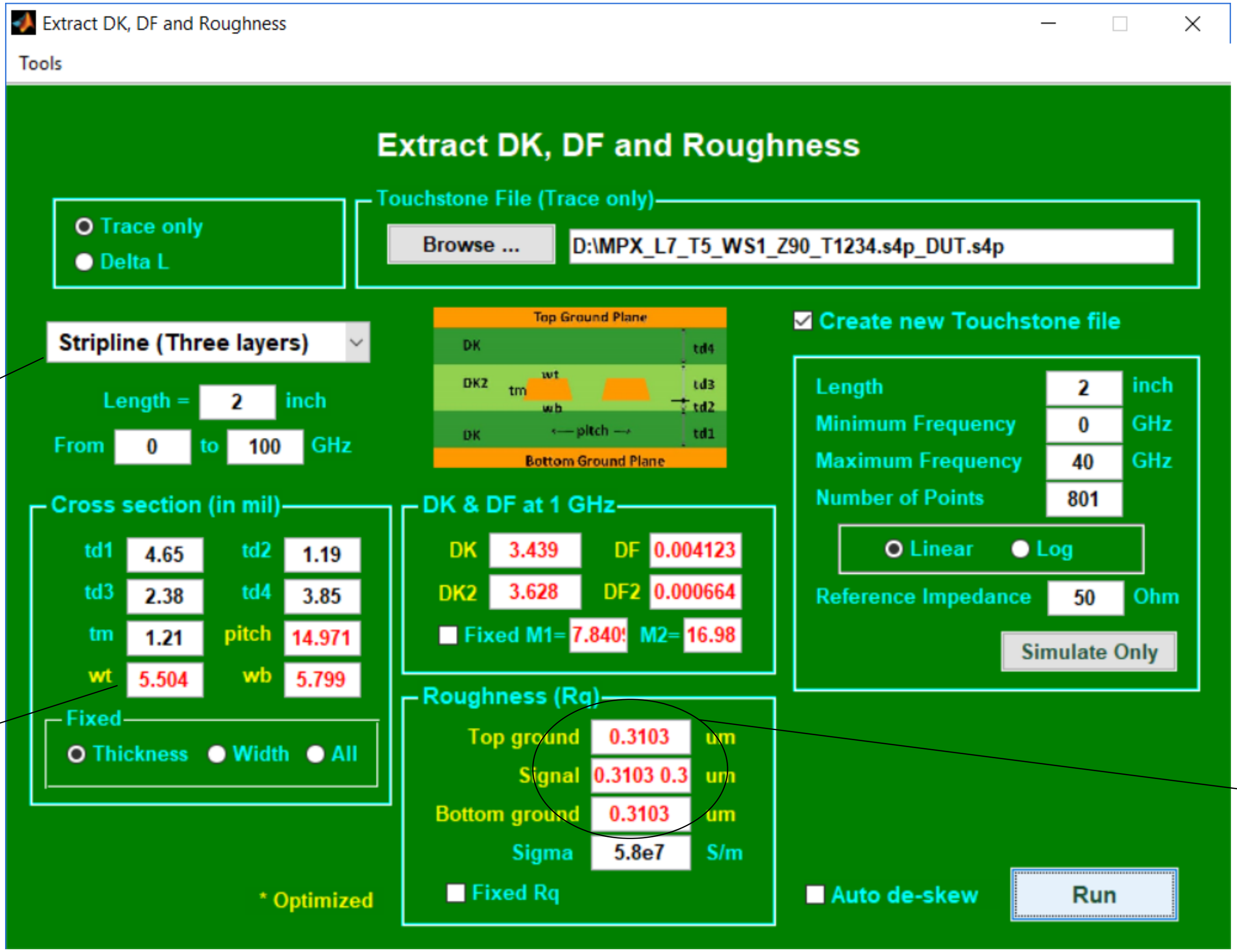
2

3

Auto de-skew

De-embedding and DUT files

DK/DF/SR extraction (from ADK)



Multiple templates

Updated after extraction

Different roughness for each surface

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To explore further…

Free seminar: "In-Situ De-embedding," 01/30/2019, 8:05 am – 8:45 am, Great America Meeting Room 2, Sponsored by Rohde & Schwarz.

Visit AtaiTec Booth #1245.

Thank you!

QUESTIONS?