DesignCon 2018

A NIST Traceable PCB Kit for Evaluating the Accuracy of De-Embedding Algorithms and Corresponding Metrics

Heidi Barnes, Keysight Technologies, heidi.barnes@keysight.com

Eric Bogatin, Teledyne LeCroy, eric.bogatin@teledynelecroy.com

José Moreira, Advantest, jose.moreira@advantest.com

Jason Ellison, The Siemon Company. jason_ellison@siemon.com

Jim Nadolny, Samtec, jim.nadolny@samtec.com

Ching-Chao Huang, Ataitec, huang@ataitec.com

Mikheil Tsiklauri, Missouri University of Science and Technology, tsiklaurim@mst.edu

Se-Jung Moon, Intel, se-jung.moon@intel.com

Volker Herrmann, Rohde and Schwarz, volker.herrmann@rohde-schwarz.com

Abstract

The constant increase in high speed digital data rates creates a corresponding decrease in design margins and the need for engineering innovations. Specifically, exploring design trade-offs to achieve reduced design margins requires accurate electrical measurements of the physical layer components that make the end-to-end digital link. The measurement accuracy provided by traditional coaxial connectors is non-existent in modern day high-density PCB interconnect designs. This has created the opportunity for innovations in measurement technology to remove custom fixturing with calibration, and the need for validation and comparison to ensure measurement accuracy.

The challenge is that there is no one solution for fixture removal, and fixture removal often requires significant engineering experience to understand the trade-offs of accuracy and calibration standard choice. In addition, most test engineers are faced with using commercial software tools that de-embed the test fixture using unknown proprietary algorithms based on a 2x-thru or 1x-reflect methodology, and traditional calibration verification standards are not readily available for these custom fixture removal techniques. Since the de-embedded measurements cannot be validated, engineers are concerned about the accuracy of the measurement of a device under test (DUT) after fixture removal. This concern is exacerbated when the DUT measurement plays a major role to determine the system margin of multi-gigabit serial link systems.

The IEEE P370 standard is being developed to address these concerns and this paper focuses on the working area defining methodologies to evaluate the accuracy of a de-embedding algorithm. The IEEE P370 standard uses both simulated and measurement data. A simulation library contains modeled fixtures, DUTs, and verification standards. Thus, the DUT after removal can be compared directly to its modeled counterpart. Conversely, a plug-and-play PCB kit connects fixtures and DUTs together using NIST traceable connections. The result is a DUT that is accessible both directly with coaxial connection and indirectly with de-embedding algorithms.

In this paper, we will present the plug and play kit for single-ended and coupled differential applications and show how it can be used to verify de-embedding algorithms with open-source 2x-thru and 1x-reflect de-embedding methodologies. Because the kit is composed of real PCB test structures, it contains all the problems associated with real PCBs, and its design is such that it allows the results of a de-embedding algorithm to be compared with the real DUT results in a NIST traceable measurement setup.

Authors' Biographies

Heidi Barnes is a Senior Application Engineer for High Speed Digital applications in the EEsof EDA Group of Agilent Technologies. Past experience includes over 6 years in signal integrity for ATE test fixtures for Verigy, an Advantest Group, and 6 years in RF/Microwave microcircuit packaging for Agilent Technologies. She rejoined Agilent Technologies in 2012, and holds a Bachelor of Science degree in electrical engineering from the California Institute of Technology.

Eric Bogatin is currently a Signal Integrity Evangelist with Teledyne LeCroy, the Dean of the Teledyne LeCroy Signal Integrity Academy, at www.beTheSignal.com. an Adjunct Professor at the University of Colorado - Boulder in the ECEE dept and the editor of the Signal Integrity Journal. Bogatin received his BS in physics from MIT and MS and PhD in physics from the University of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. He has written six technical books in the field and presented classes and lectures on signal integrity world wide.

Jose Moreira is a senior staff engineer in the test cell innovations team of the SOC business unit at Advantest in Böblingen, Germany. He focuses on the challenges of testing high-speed digital devices especially in the area of test fixture design, signal integrity, jitter testing and focus calibration. He joined Agilent Technologies in 2001 (later Verigy and in 2011 acquired by Advantest) and holds a Master of Science degree in Electrical and Computer Engineering from the Instituto Superior Técnico, Lisbon University, Portugal. He is a senior member of the IEEE and co-author of the book "An Engineer's Guide to Automated Testing of High-Speed Digital Interfaces".

Jason Ellison is a Signal Integrity Engineer employed by The Siemon Company of Watertown Connecticut. Jason develops cable assemblies, connectors and automated test methodologies to support current and next generation data centers. He has graduated with a Masters of Electrical Engineering Science from Penn State University, is a member of the IEEE, and has served as a Fire Direction Center Sergeant in the US Army's 109th Field Artillery, 28th Division.

Jim Nadolny received his BSEE from the University of Connecticut in 1984 and an MSEE from the University of New Mexico in 1992. He began his career focused on EMI design and analysis at the system and component levels for military and commercial platforms. His focus then shifted to signal integrity analysis of multi-gigabit data transmission. Jim is active within the technical community currently serving as a Technical Group chairman for IEEE P370, a standard focused on precision measurements of passive interconnect components. Jim is a frequent presenter at DesignCon with Best Paper awards in 2004, 2008 and 2012 and has over 25 peer reviewed publications. At Samtec, Jim tracks technology trajectories via industry standards, MSAs and other collaborations.

Ching-Chao Huang, founder and president of AtaiTec Corporation, has more than 30 years of high-speed design and SI software development experience. He was advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member and he pioneered In-Situ De-embedding (ISD) for causal and accurate de-embedding. He received his BSEE from National Taiwan University and MSEE and PhD from Ohio State University.

Mikheil Tsiklauri is a research professor from Missouri University of Science and Technology. He received the B.S., M.S., and Ph.D. degrees in applied mathematics from Tbilisi State University, Tbilisi, Georgia, in 1998, 2000, and 2003, respectively. From 2000 to 2012, he was with Tbilisi State University. His research interests include applied mathematics, algorithms, mathematical modeling and software development for EM problems. Currently Mikheil is serving as a Technical Group 3 co-chair for IEEE P370, a standard focused on S-Parameters Integrity and Quality.

Se-Jung Moon is a Senior Hardware Engineer at Intel Corporation. She leads the signal integrity effort in enabling, designing and evaluating high-speed connectors and cables for DCG (Data Center Group) platform development. She received her PhD in ECE from University of Illinois at Urbana Champaign and her master in physics and BSEE in ECE from Seoul National University.

Volker Herrmann is received the Dipl. Ing. (FH) degree from the University of Applied Science of Mannheim in 2000. In 2010, he joined Rohde & Schwarz as an application engineer supporting vector networks analyzers. His previous positions included application engineer and product manager for wireless products at semiconductor companies.

Introduction

Test fixture de-embedding is a critical step in the accurate measurement of a Device Under Test (DUT) when it cannot be directly connected to the calibrated reference location of the measuring instrument [1]. However, it can be indirectly measured using de-embedding methods such as multiline TRL [2], iTRL [3] or 2x-thru de-embedding [4-7].

Figure 1 shows an example of a simple test fixture for a SPDT solid state relay with a 2x-thru de-embedding structure, and the measured and de-embedded S-parameters for one of the relay signal paths. The results show that even on a small high-performance test fixture, de-embedding is required to obtain the real DUT performance.

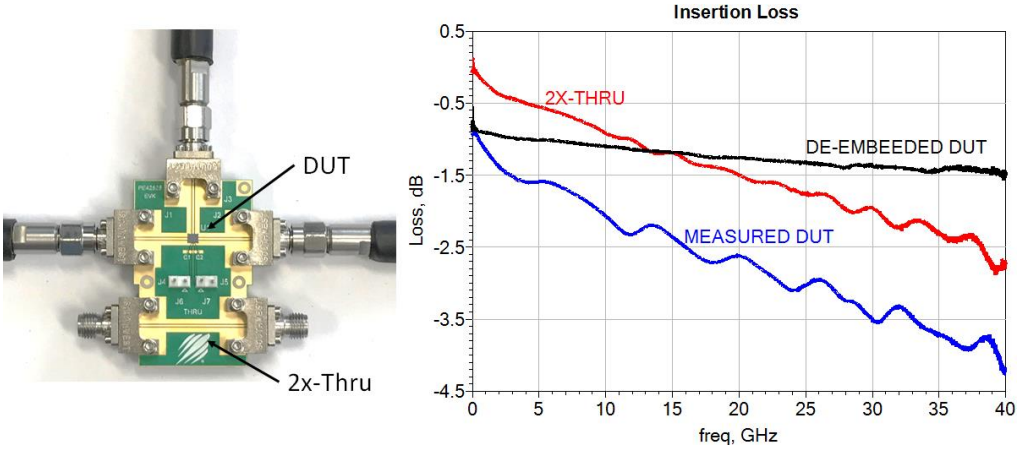

Figure 1: Example of a test fixture for a SPDT solid state switch DUT with a 2x-thru de-embedding structure.

De-embedding methodologies only work properly if the de-embedding structures and the test fixtures have a certain quality. Figure 2 shows two examples of quality criteria related to the test fixture shown in Figure 1.

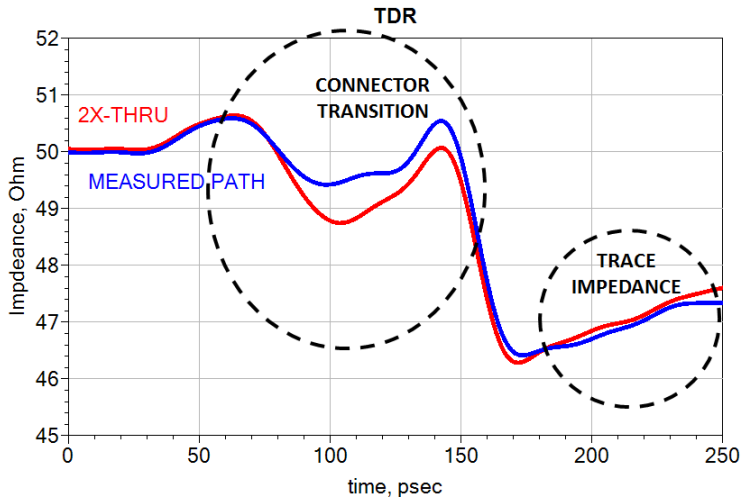

Figure 2: TDR comparison of the measured 2x-thru with one of the test fixture DUT relay paths.

The first criteria is the connector transition of the 2x-thru and the test fixture DUT paths are similar. The second criteria is the trace impedance of the 2x-thru and the test fixture DUT paths are also similar. The question is, how similar they should be to achieve a certain de-embedding accuracy? This is a key topic being addressed by the IEEE P370 standard working group [8].

Currently, multiple commercial software packages provide support for 2x-thru de-embedding (e.g. [9,10,11]). The complete details of the de-embedding algorithms in each of these commercial tools is confidential since they have developed IP to improve the de-embedding results. From a user perspective, these de-embedding algorithms are basically a black box making it difficult to analyze the accuracy of these algorithms in different conditions. This is another topic that the IEEE P370 working group [8] is addressing. Two approaches are being followed. The first approach uses simulation generated S-parameters for evaluating the de-embedding algorithms accuracy [12]. The strength of this approach is the ability to easily modify any parameter of a given test fixture signal path model and observe its impact on the de-embedding algorithm accuracy.

The second approach uses a kit composed of multiple PCB test coupons connected together using calibration grade adapters [13]. This approach, although not as flexible as the simulation based one, uses real hardware. This means that all the added challenges, like the VNA calibration and measurement setup, are included in the data provided to the de-embedding algorithm. Both approaches are complimentary and needed for evaluating which test fixture parameters are critical for determining the accuracy of the de-embedding algorithms.

This paper presents the detailed methodology of using a real PCB kit for evaluating the accuracy of 2x-thru de-embedding algorithms for both single-ended and differential coupled scenarios. In addition, we will show how the kit can be used to evaluate the 1x-reflect methodology. We will also discuss a possible approach for a PCB kit to evaluate crosstalk de-embedding.

In the next sections, we will first provide a high-level overview of the 2x-thru and 1x-reflect de-embedding methodologies followed by a description of the methodology used on the PCB kit to allow an accurate evaluation of the de-embedding algorithm accuracy. We will follow up with a presentation of the single-ended and differential coupled kits and corresponding results. The de-embedding algorithm used in this paper, is a non-commercial MATLAB based script, since the objective is to present how the methodology works and not evaluate the currently available commercial de-embedding software packages.

We will also present a short discussion of a possible PCB kit to evaluate crosstalk de-embedding algorithms based on a 2x-thru (spiderleg) approach and a high-level discussion on the challenges of S-parameter quality. This is important since an accurate de-embedding result does not guarantee that the resulting S-parameter file has the needed quality to be used in, for example, time domain simulations.

2x-Thru Based De-embedding

The algorithm as described in one of the early papers [4] makes use of the symmetry of the test fixture on either side of the DUT to create a 2x-thru. This back-to-back connection of the fixture A on one side and fixture A' on the other side of the DUT makes it possible to extract the fixture's S-parameters. Commercially available tools are now quite sophisticated in the mathematical methods of "splitting" the fixture 2x-thru S-parameters into the cascade of two S-parameters.

Here, we explain the 2x-thru methodology. This is not intended to divulge the trade secrets of commercial tools or make claim that this method replaces such products. Instead, the purpose is to educate users with the general philosophy of the method grounded with engineering references. Consider a signal flow graph of a reciprocal 2x-thru structure in Figure 3 where each half of the 2x-thru is assumed to be the mirror of the other [14]. By examination, there are three unknowns that make up the test fixture model: e_{00}, e_{11}, and e_{01}.

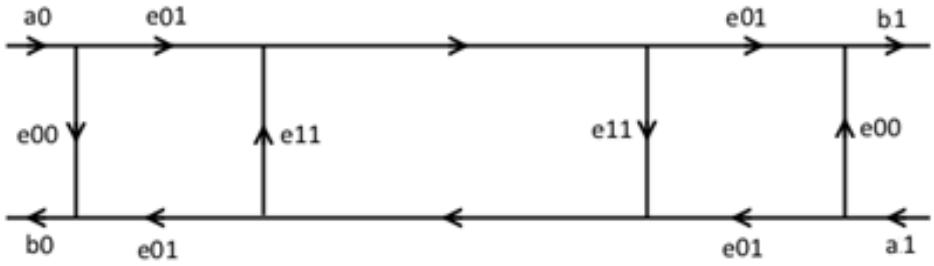

Figure 3: 2x-thru signal flow graph.

If the S-parameters of the 2x-thru are S_{ij}, solving this signal flow graph for the S-parameters of the 2x-thru in terms of the test fixture model yields two equations:

$$S_{11} = \frac{b_0}{a_0}\Big|_{a_1=0} = e_{00} + \frac{e_{11}e_{01}^2}{1 - e_{11}^2}$$

$$S_{21} = \frac{b_1}{a_0}\Big|_{a_1=0} = \frac{e_{01}^2}{1 - e_{11}^2}$$

Completely calculating the test fixture model requires another equation or known variable. This method finds another variable by converting S_{11} and S_{21} from the frequency-domain into the time-domain. Find e_{00} in the time-domain by using a window function on the time-domain S_{11} that truncates the numerical data at the middle of the test fixture [15]. Since time of flight of a reflection at a given point is twice the time it takes to reach that point, the mid-point of the reflection is the 50% crossing of S_{21} step response or the maximum value of S_{21} impulse response. Figure 4 shows an example test fixture time domain data and a rectangular window function applied with the proper position and width. Finally, convert the time domain e_{00} into the frequency domain to find the auxiliary variable.

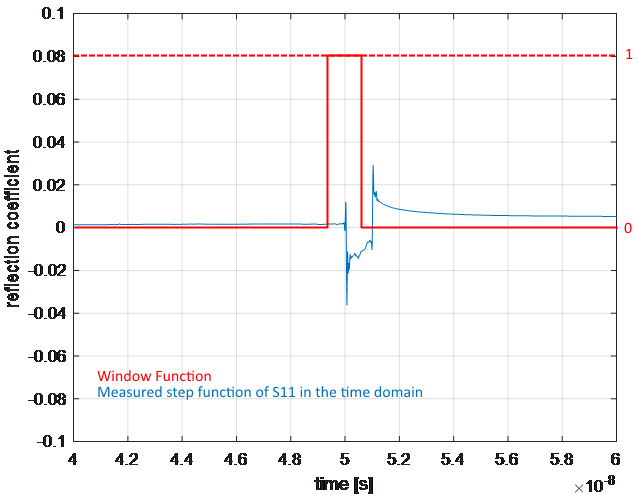

Figure 4: A window function which truncates at the middle of a test fixture and a test fixture step response.

Now, there are two equations and two unknowns and finding the complete solution is possible. Figure 5 shows this process in a block diagram to help the reader understand the process flow.

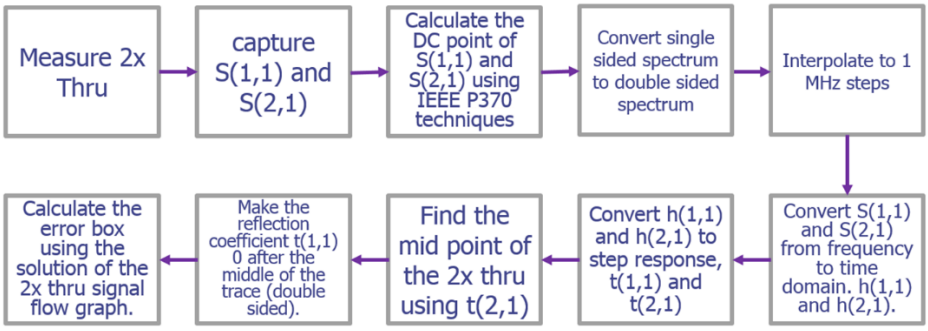

Figure 5: High-level block diagram of a 2x-thru method implementation.

As written, the method extracts the test fixture model in the left-hand side of the block diagram in Figure 5. Perform this process a second time while replacing S_{11} with S_{22} to calculate the test fixture model in the right-hand side of the signal flow graph in Figure 3. This method robustly handles impedance discontinuities, relatively large test fixtures, and reflections as high as -5 dB. However, nominal transmission line variations greater than 5% between the calibration 2x-thru and the in-situ fixture attached to the DUT will significantly degrade the de-embedding accuracy.

Impedance Correction

In most test fixture cases, the 2x-thru will be a calibration test fixture with connectors and a PCB trace that is twice as long as the signal trace on the fixture connected to the DUT. The 2x-thru and DUT fixture impedance can be different due to manufacturing process variations, and this difference is a source of error. To minimize this error, an impedance correction algorithm [19] changes the 2x-thru impedance to match the DUT fixture impedance.

The algorithm considers the frequency dependent propagation constant of the 2x-thru constant with respect to position. This assumption enables the extraction of the propagation constant from the attenuation and phase of the 2x-thru transmission S-parameters. In one implementation, the algorithm makes a new 2x-thru by concatenating uniform transmission lines that match the impedance of the trace until the impedance of a test fixture model is perfectly matched to the DUT fixture (Figure 6).

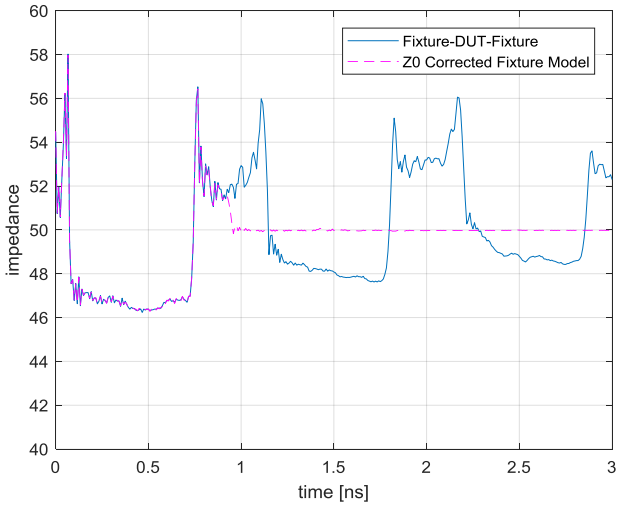

Figure 6: Fixture-DUT-fixture and test fixture model impedance after the impedance correction algorithm.

1x-Reflect Based De-Embedding

There are some applications where using a 2x-thru de-embedding approach can be very challenging (e.g., test fixtures with sockets [16], packages or on wafer measurements [17]). Also, sometimes the PCB designer did not plan ahead and forgot to include a 2x-thru de-embedding structure. In these cases, the only option is to use 1x-reflect de-embedding with an open or short test structure [18]. In the case of socket based test fixture, the open-ended test structure can be obtained by simply removing DUT from the socket. Figure 7 shows the signal flow graph of 1x-reflect where Γ=+1 (or -1) for reflection from the open (or short) end.

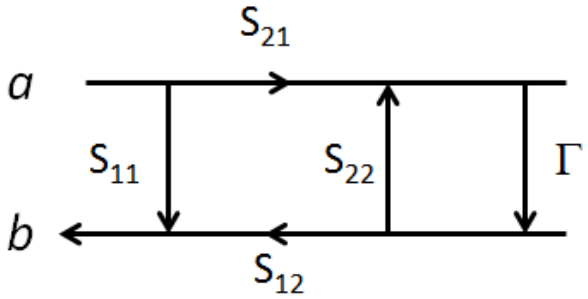

Figure 7: Signal flow graph of 1x-reflect.

The measured quantity $S_{11}^{open\ or\ short}$ can be written as:

$$S_{11}^{\text{open or short}} = \frac{b}{a} = S_{11} + \frac{S_{12}S_{21}\Gamma}{1 - S_{22}\Gamma} \tag{1}$$

where S_{11}, S_{12}, S_{21} and S_{22} are to be solved.

It is quite a challenge to solve so many unknowns with only one equation. Several commercial tools (e.g., ISD [9,19], PLTS [10,18] and SFD [11]) are available to address such 1x-reflect challenge with the aid of frequency-domain and time-domain transformations. Figure 8 shows a simplified high-level block diagram for a 1x-reflect de-embedding method implementation. Note that after the last step in the diagram, commercial tools might apply further algorithms to further refine the results that are not publicly available.

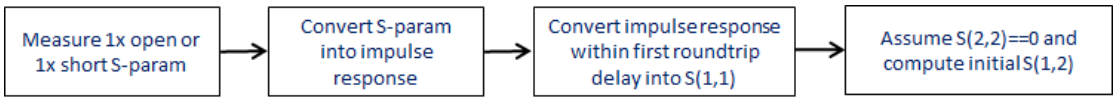

Figure 8: Simplified high-level block diagram of a 1x-reflect method implementation.

As shown in Figure 9, S_{11}, S_{12}, S_{21} and S_{22} are related to the impulse response of $S_{11}^{open\ or\ short}$ during and after the initial round-trip delay. It is possible to fine-tune their results through numerical optimization [16]. For good accuracy, 1x-open and/or 1x-short measurements must have minimal fringing field effects at the open and/or short ends.

Note that the 1x-open structure is usually more available than the 1x-short structure. In a socketed test fixture, the 1x-reflect algorithm can be readily applied using an open corresponding to no DUT inserted in the socket. Clearly for small pitch applications at high-frequency, the fringing field effects will be significant and the open socket will deviate from an ideal open.

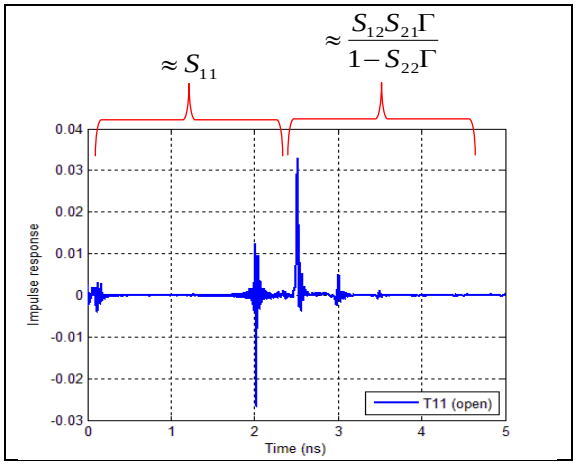

Figure 9. Identifying S parameters from impulse response of 1x-reflect.

When both 1x-open and 1x-short coupons are available, S parameters of an "effective" symmetric 2x-thru can be derived as follows [20]:

$$[S]^{2x} = \begin{bmatrix} S_{11}^{2x} & S_{12}^{2x} \\ S_{12}^{2x} & S_{11}^{2x} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} S_{11}^{open} - S_{11}^{short} & S_{11}^{open} + S_{11}^{short} \\ S_{11}^{open} + S_{11}^{short} & S_{11}^{open} - S_{11}^{short} \end{bmatrix} \quad (2)$$

Then, all algorithms that were used for 2x-thru de-embedding are directly applicable to 1x-open and 1x-short de-embedding. The challenge is to have both 1x-open and 1x-short measurements available and with both open and short being close to ideal.

De-Embedding Accuracy Metrics

To access the accuracy of a de-embedding algorithm it is necessary to have a metric that provides the error between the true DUT S-parameters and the computed de-embedded S-parameters. This metric can only be used in cases where the true DUT S-parameters are known (e.g. simulation or the proposed PCB kit methodology). In the IEEE P370 working group one approach under discussion is to use the error vector of the S-parameters at each frequency to determine error since it would then include not only the error in the magnitude but also in the phase. Specifically, two types of error metrics are proposed: a relative error and an absolute error metric as described in the following equations [12,21]:

Absolute error function:

$$EF_{ij}(f) = \mathrm{mag}\left[S_{ij}^{A}(f) - S_{ij}^{B}(f)\right]$$

Relative error function:

$$rEF_{ij} = \frac{\mathrm{mag}\left[EF_{ij}(f)\right]}{0.5 \times \mathrm{mag}\left[S_{ij}^{A}(f) + S_{ij}^{B}(f)\right]}$$

These two terms are magnitudes. The absolute error function is the absolute vector difference of the two S-parameter vectors. The relative error function is the relative magnitude of the vector difference to the average value of the S-parameter models. The error function is shown graphically in Figure 10.

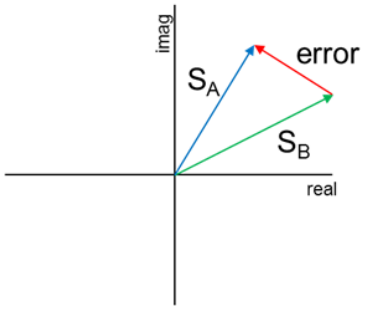

Figure 10: Graphical example of the definition of the error function. It is a complex number and calculated at each frequency.

The open question is which error metric to use when comparing for example the insertion loss or the return loss and which error value represents a good de-embedding accuracy. These are topics under discussion on the P370 standard [8]. Currently most users use the relative error metric for the insertion loss and the absolute error metric for the return loss.

PCB Kit Methodology

To develop a physical vehicle to evaluate the accuracy of de-embedding algorithms, one critical requirement is that the de-embedding reference plane be a well-behaved interface without any discontinuities. An ideal candidate would be a calibration grade adapter. Combining this idea with the usage of individual PCB coupons with edge connectors for the test fixture and DUT we come to the methodology described in Figure 11 [13]. The DUT is connected to each side of the test fixture using a combination of male/male and male/female calibration grade adapters with the de-embedding reference plane set at their connection point. The challenge is how to measure the 2x-thru since the adapters will not mate as shown in Figure 12. The solution is to perform an adapter swap, switching the male/male adapter to a male/female adapter. This only works if the adapters are assumed to have the same exact performance, especially that they are phase matched as is typical for calibration grade adapters.

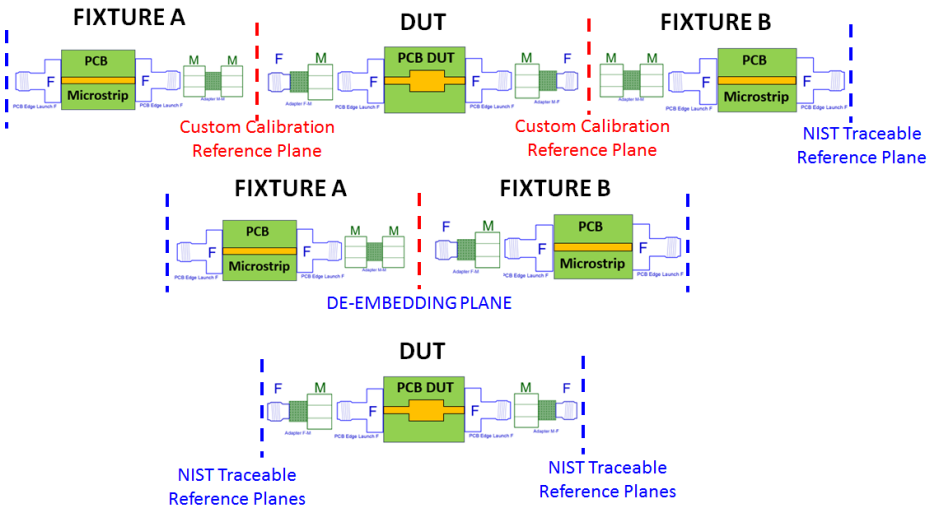

Figure 11: De-embedding algorithm verification concept for a 2x-thru based de-embedding approach.

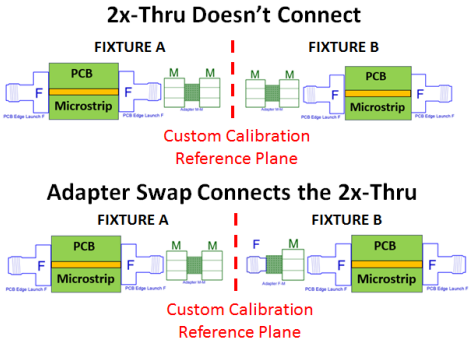

Figure 12: Solving the 2x-thru mating challenge by swapping connector gender.

The concept can be also applied to the evaluation of a 1x-reflect based de-embedding algorithm as shown in Figure 13. Note also that although in Figure 11 symmetrical test fixtures are used, this methodology can also be applied to evaluate de-embedding of unsymmetrical test fixtures where two different 2x-thru are needed as shown in [22].

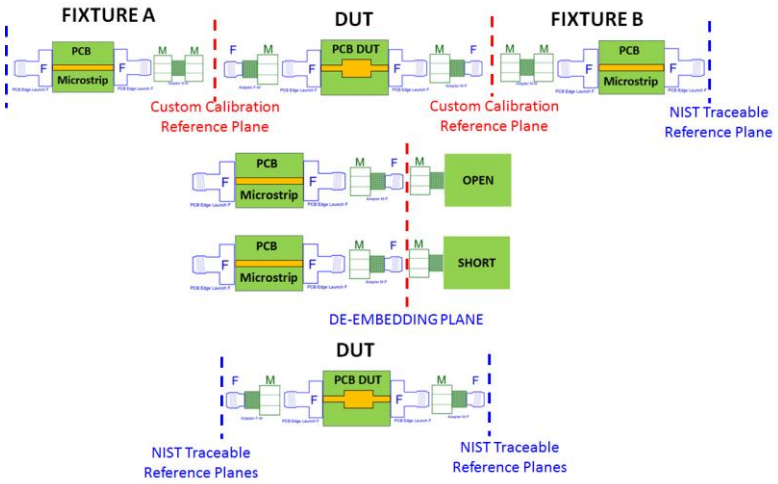

Figure 13: De-embedding algorithm verification concept for a 1x-reflect based de-embedding approach.

NIST Traceability

By using a calibrated VNA for each measurement operation we have a NIST traceable measurement of each configuration. The one critical point for the NIST traceability of the proposed methodology is the adapter swapping operation described in the previous section. We need to quantify the maximum error from this adapter swapping especially in regard to the connector electrical delay. One can directly measure each adapter by utilizing a mechanical calibration kit to do two separate calibrations, an insertable calibration for the M/F adapter, and a non-insertable calibration for the M/M adapter. However as simpler approach is to measure the adapter with a known mechanical calibration kit short standard (male or female)

attached to the end of each adapter as shown on Figure 14. This only requires one calibration set-up for the VNA ports.

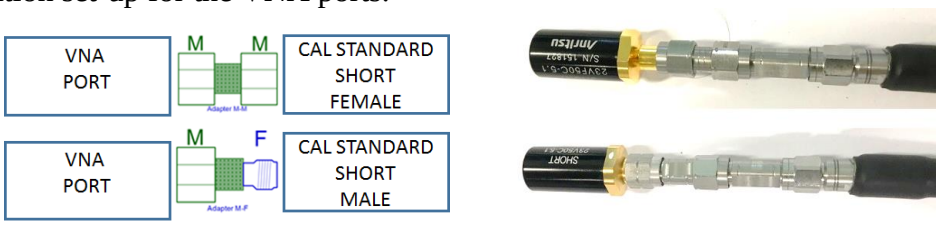

Figure 14: Measuring the adapter swap error.

The male and female short calibration standards in a mechanical calibration kit are NIST traceable standards which allows one to use the traceability of the mechanical calibration kit data to bound the error from the difference between the male and female short standards. Figure 15 shows the measured return loss, phase and computed TDR waveform of calibration grade male/female and male/male 1.85 mm adapters using a male and a female short calibration kit standard. The absolute vector difference between both adapters was also computed.

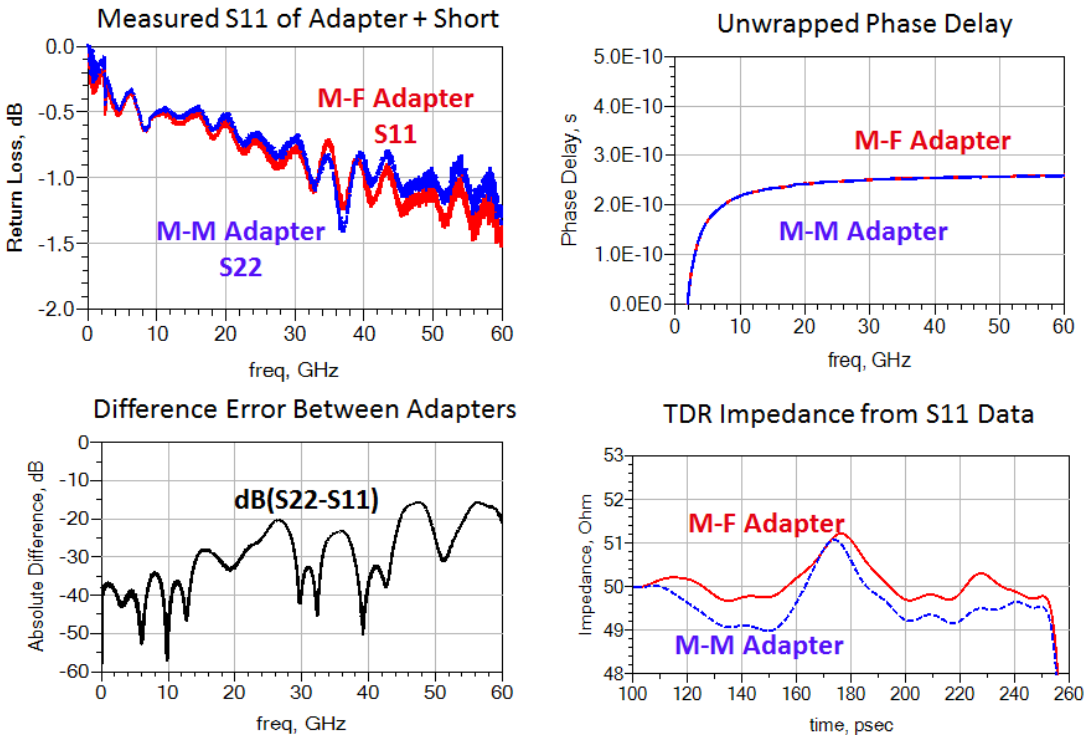

Figure 15: Measured return loss, phase delay and computed TDR for the M/M and M/F adapters with calibration grade male and female shorts and computed absolute error.

The measured data in Figure 15, show how well these low loss measurement grade adapters are matched. The unwrapped phase delay shows very little difference, and the biggest contribution to the absolute error is in the impedance variation between the M-F and F-F connector interface. This data can be used to understand the limits of the absolute error between the direct measurement of the DUT with this Plug and Play kit and the DUT after fixture removal.

Single-Ended Kit

The methodology described in the previous section was implemented in a kit composed of two DUTs and three types of test fixtures. The chosen DUTs were a 6 cm microstrip which represents a very simple DUT and a Beatty standard [23] which provides a DUT with a strong series resonance. For the test fixtures the choices were a simple 6 cm test fixture, a test fixture with 2 optimized vias in series and a test fixture with a target impedance that is 105% of the nominal impedance. The test fixtures are intended to stress different aspects of the de-embedding algorithms.

Figure 16 shows a picture of the kit with 1.85 mm edge mounted connectors to be able to reach a 65 GHz measurement bandwidth. The kit was implemented on a Rogers 4003 dielectric with a NiAu plating (minimum of 75 µm Au thickness). The design trace width is 17.3 mil. Figure 17 shows the connector footprint and a 1.85 mm connector assembled to the edge of the test coupon.

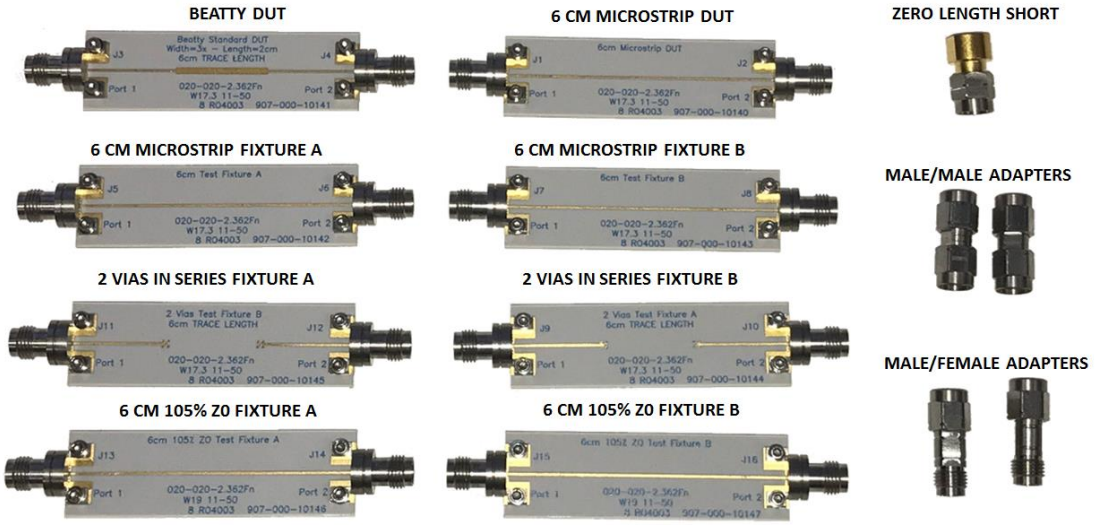

Figure 16: Single-ended kit picture.

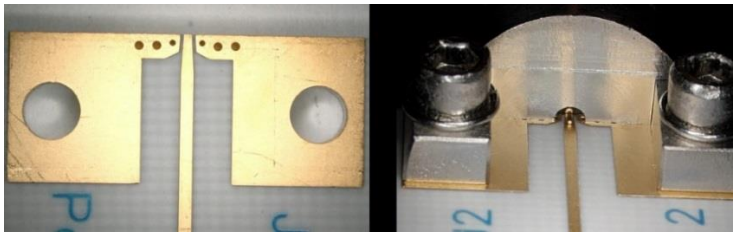

Figure 17: Connector footprint and assembled 1.85 mm connector.

Figure 18 shows the computed TDR (from the measured S-parameters) for the kit coupons. For the measured kit the nominal impedance is ~46 Ohms with the Beatty standard at ~22 Ohms and the 105% nominal impedance coupons at 44 Ohms. This means the kit impedance difference correspond to the target value especially the 2 Ohm difference for the 105% nominal impedance test coupons.

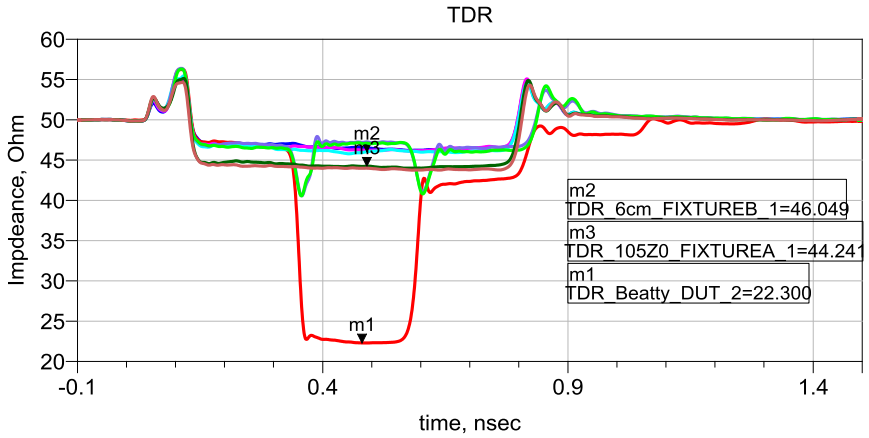

Figure 18: TDR results for the different PCB test coupons in the kit.

As described previously in Figure 11, the reference measurement of the DUT needs to be performed with a male/female adapter on each side as shown in Figure 19. The results for both DUTs in the kit are presented in Figure 20. All measurements were performed using 1.85 mm edge connectors and a VNA measurement range of 6 MHz to 60 GHz with 10000 points and an IF bandwidth of 1 KHz. The VNA was calibrated to the end of the coaxial cables with the proper calibration unit.

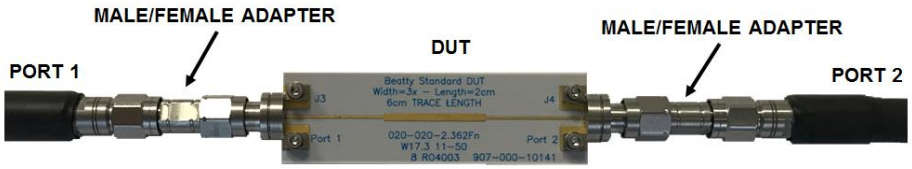

Figure 19: Setup example picture for measuring the DUT.

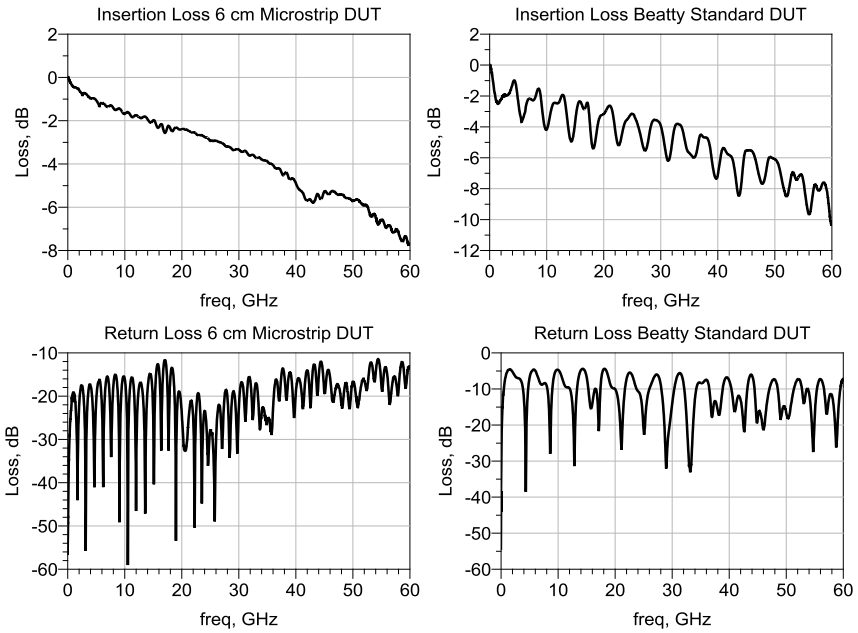

Figure 20: Measured S-Parameters for the 6 cm microstrip and Beatty standard DUTs (including the male/female adapters).

The second important series of measurements are the 2x-thru measurements for the three types of test fixtures as shown in Figure 21 for the two vias in series test fixture. The results are presented in Figure 22.

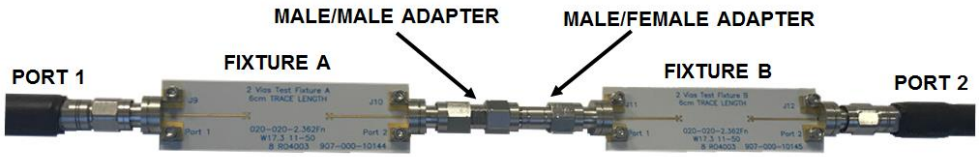

Figure 21: Setup example picture for measuring the 2x-thru of the test fixture.

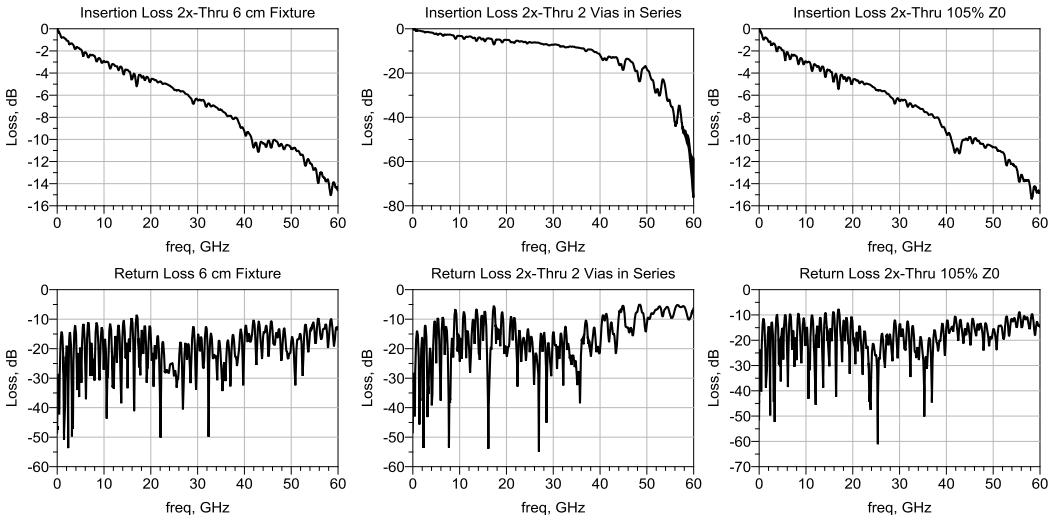

Figure 22: Measured S-Parameters of the 2x-thru for the three different types of test fixtures.

One usual metric used to evaluate the possible de-embedding range for a given test fixture 2x-thru, is to measure the separation between the insertion loss and return loss as shown in Figure 23 for the two vias in series 2x-thru case. Different rules have been proposed including a minimum of 5 dB separation (~9 GHz in Figure 23) or simply the point where the insertion and return loss cross (~40 GHz in Figure 23).

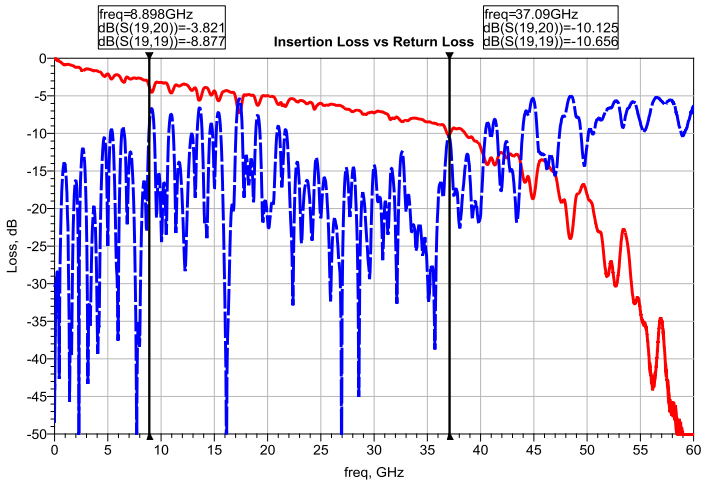

Figure 23: Measuring the separation between the insertion and return loss for the 2 vias in series 2x-thru.

If a 1x-reflect based de-embedding methodology is used, then as described in Figure 13 and shown in Figure 24, it is necessary to measure the return loss with an open and short configuration.

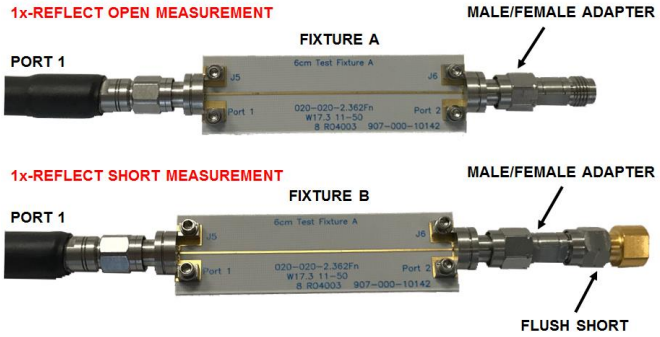

Figure 24: Setup example picture for measuring open and short for the 1x-reflect methodology.

Now that we have the required measured data for 2x-thru or 1x-reflect based de-embedding we can now measure the DUT with the test fixture as shown in Figure 25. Figure 26 shows the results for both DUTs with the 6 cm microstrip test fixture and the two vias in series test fixture.

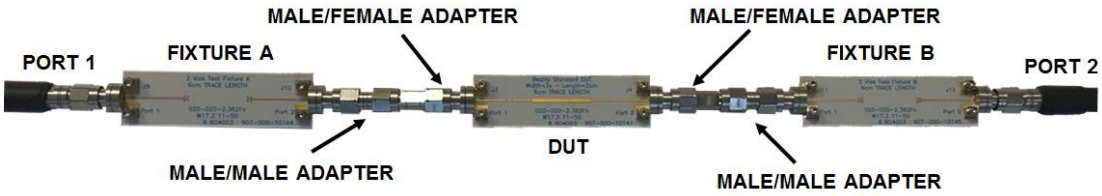

Figure 25: Setup example picture for measuring the DUT plus the test fixture.

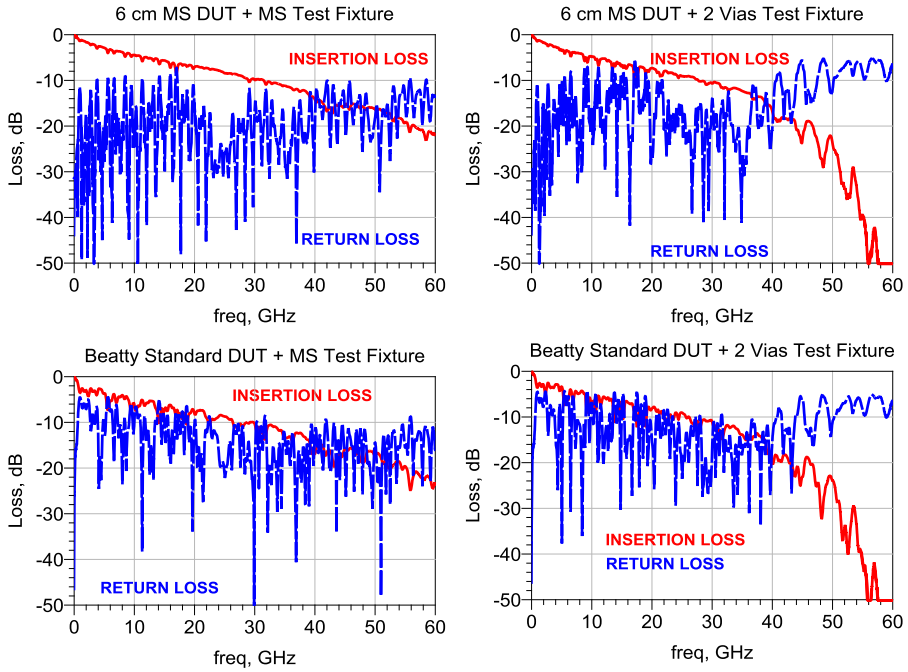

Figure 26: Measured S-Parameters for the two DUTs plus the different test fixtures.

2x-Thru De-Embedding Results

Now that we have all the required measured data, we can apply a de-embedding algorithm. The de-embedding algorithm used here is a MATLAB non-commercial toolset developed by Jason Ellison in the context of the P370 standard [24]. This toolset is intended to be used as a free de-embedding tool for engineers to understand the basics and challenges of S-parameter de-embedding, and has been developed without proprietary intellectual property. This means this toolset will yield less accurate results than commercial software packages. However, the objective of the paper is to demonstrate a methodology to assess a de-embedding algorithm accuracy, for which this toolset is more than enough

Figure 27 shows the obtained 2x-thru de-embedding results for the 6 cm microstrip DUT using the 6 cm test fixture and also the corresponding error metrics when comparing the de-embedding results with the original DUT S-parameters. In the error plots, -20 dB corresponds to a 10% error which is usually seen as a threshold for a good de-embedding. In this case for the 6 cm microstrip DUT and test fixture we see a good de-embedding all the way till almost 60 GHz if we use the absolute error metric in the analysis of the return loss error. The same applies for the de-embedding with the Beatty standard DUT shown in Figure 28.

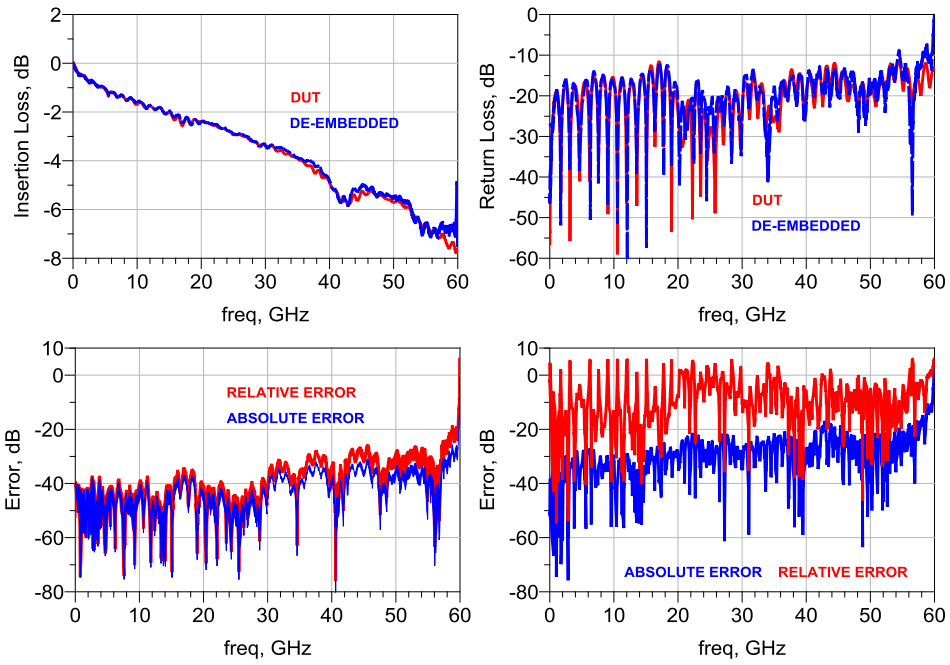

Figure 27: De-embedding results for the 6 cm microstrip DUT with the 6 cm microstrip test fixture using 2x-thru based de-embedding.

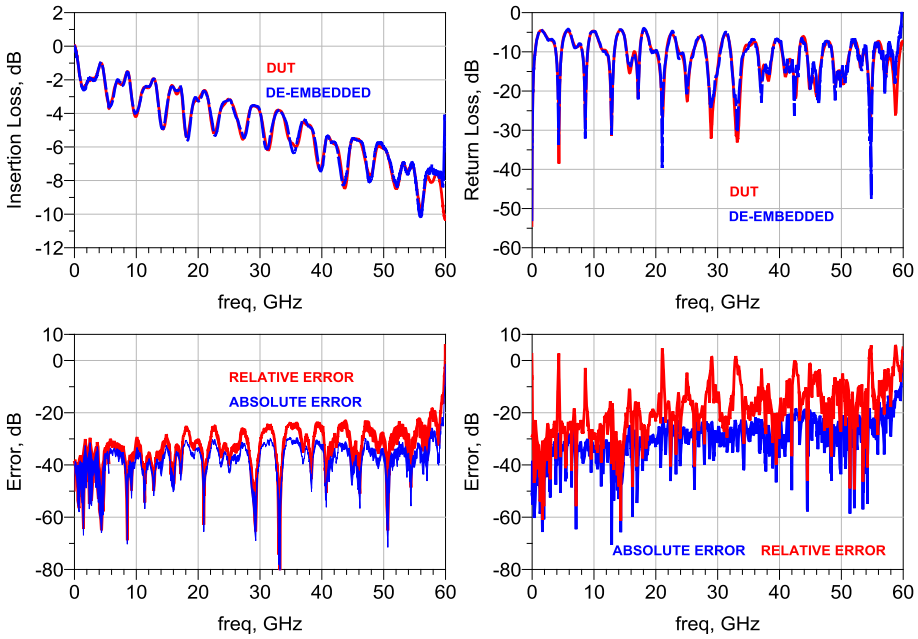

Figure 28: De-embedding results for the Beatty standard DUT with the 6 cm microstrip test fixture using 2x-thru based de-embedding.

Figure 29 shows the results for the 6 cm microstrip DUT but now with the 2 vias in series test fixture. Comparing with the results in Figure 23, one can observer that the 5 dB separation rule between the insertion and return loss is a too stringent requirement for good de-embedding as demonstrated on this example.

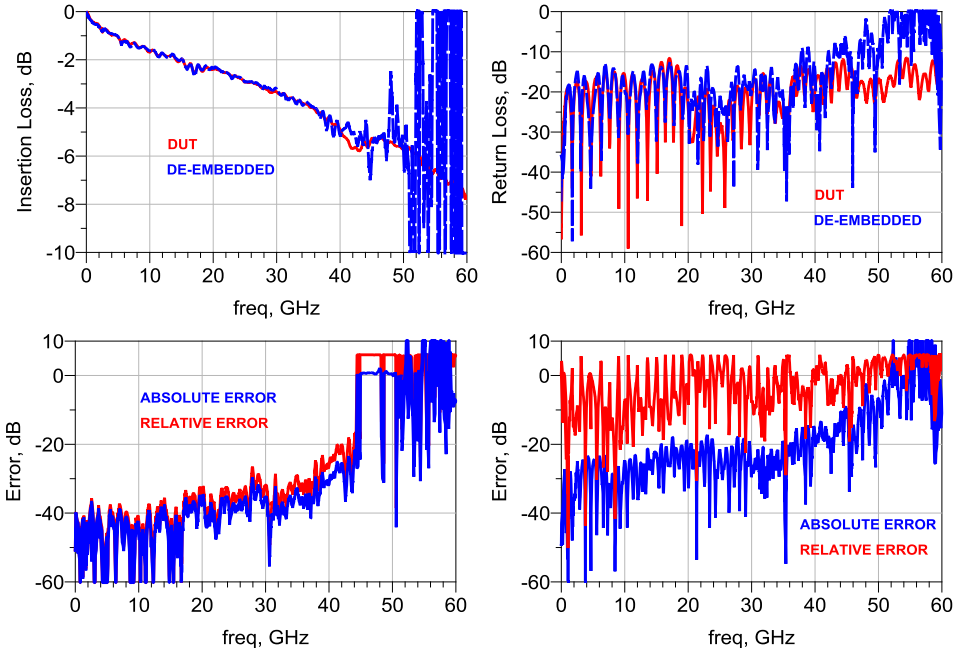

Figure 29: De-embedding results for the 6 cm microstrip DUT with the two vias in series test fixture using 2x-thru based de-embedding.

There is one easy test that can be performed to estimate the accuracy of the de-embedding procedure based on the measured 2x-thru data and a specific de-

embedding algorithm. Basically, we apply the 2x-thru to itself in what is called self de-embedding. This approach assumes a perfect DUT with zero loss and delay. Figure 30 shows the self de-embedding results for the 2x-thru composed of the 2 vias in series test fixtures. Note that the results correlate with Figure 29 where we obtained good de-embedding (less than 10% error) almost to 40 GHz.

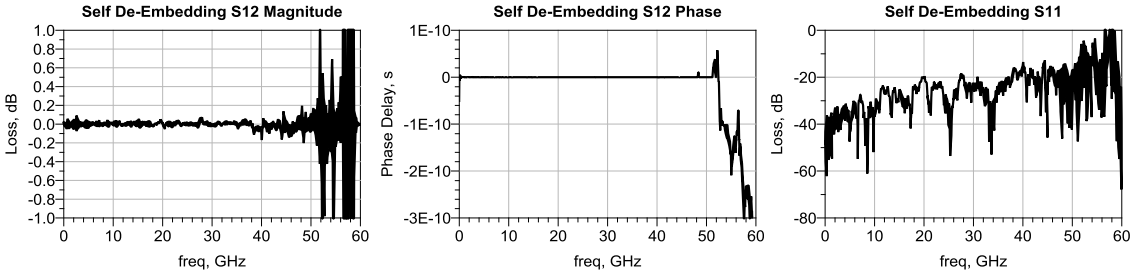

Figure 30: Self de-embedding results for the 2 vias in series 2x-thru.

1x-Reflect De-Embedding Results

Figure 31 shows the de-embedding results for the 6 cm microstrip DUT with 6 cm microstrip using the 1x-reflect de-embedding methodology. The de-embedding accuracy results are worse than the ones obtained with the 2x-thru methodology shown in Figure 27. This is expected since although the 1x-reflect methodology is easier to use, it depends strongly on the quality of the open and short. Figure 32 shows an analysis of the test fixture short measurement where the electrical delay of the fixture plus the male/female adapter was de-embedded. It shows that the short no longer behaves as a short at the higher frequencies as expected. Note that unlike on a calibration kit, the short is assumed to be a perfect short since no short model is provided to the de-embedding algorithm.

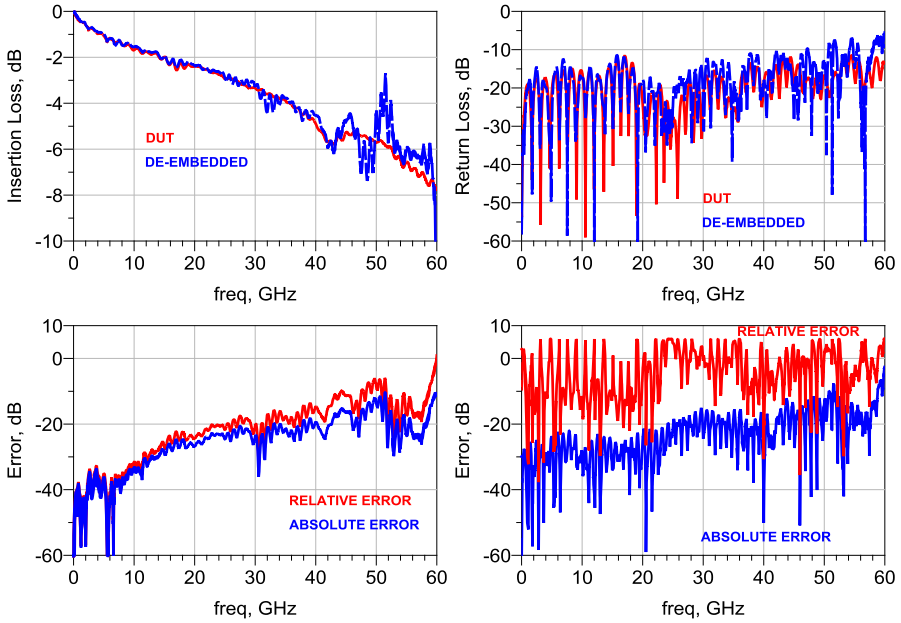

Figure 31: 1x-reflect results for the 6 cm microstrip DUT with the 6 cm test fixture.

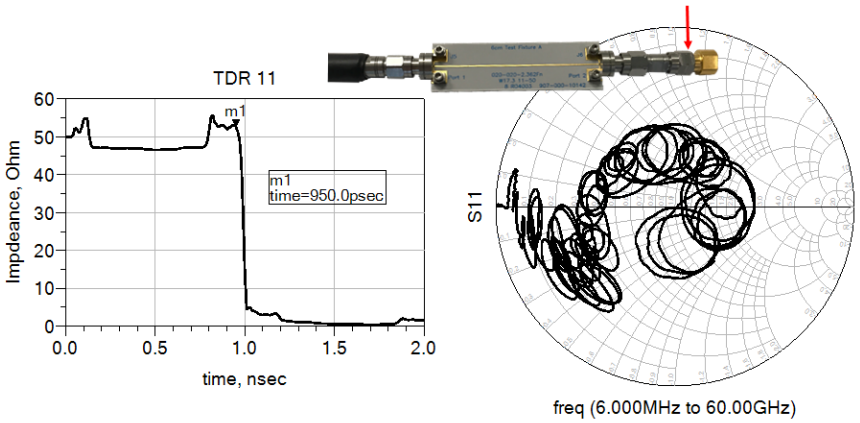

Figure 32: Checking the quality of the short at the end of the test fixture used for the 1x-reflect de-embedding.

In Figure 33 we show the de-embedding results when using the 2x-thru obtained with the 105% Zo test fixtures instead of the correct 2x-thru for the 6 cm microstrip DUT. This cases represents the situation where the 2x-thru and the DUT test fixture traces have a different impedance (e.g. due to process variation). In this case 2 Ohms. The results show that the insertion and return loss have a good matching till 40 GHz but the computed error is in fact high. This is due to the phase error as shown in Figure 34. To address this impedance difference challenge, some de-embedding algorithms include an impedance correction algorithm which provide more accurate results when looking in the time domain as shown in Figure 35. But note that this impedance correction algorithm will not correct the phase error.

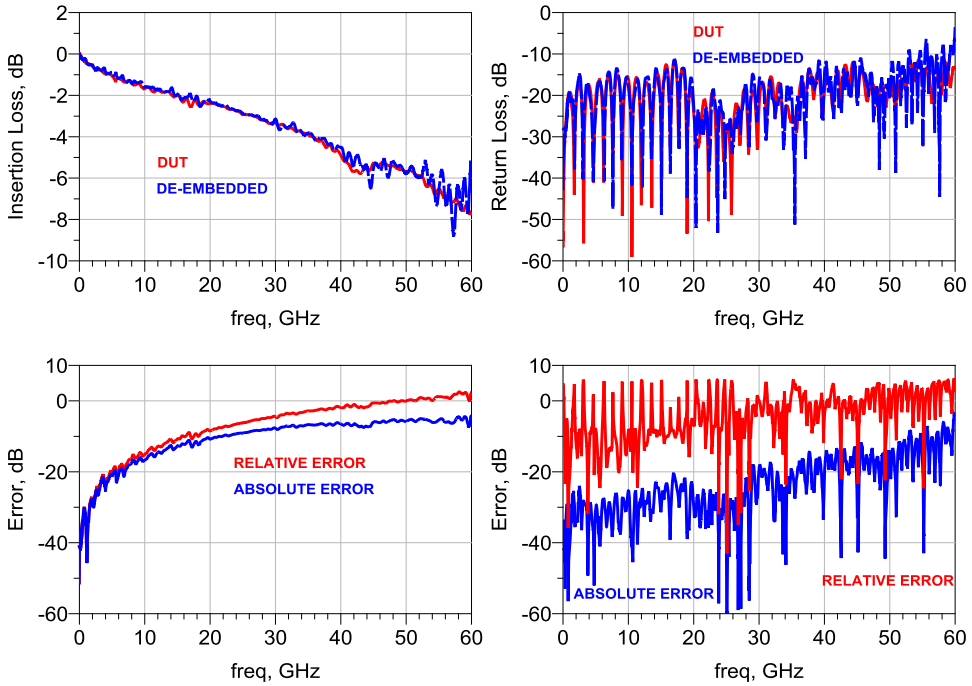

Figure 33: De-embedding results for the 6 cm microstrip DUT with the 6 cm 105% nominal impedance microstrip test fixture using 2x-thru based de-embedding.

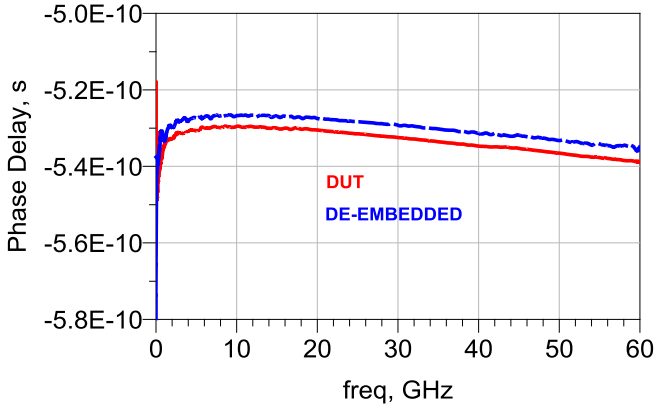

Figure 34: De-embedding results for the 6 cm microstrip DUT with the 6 cm microstrip test fixture using 2x-thru based de-embedding.

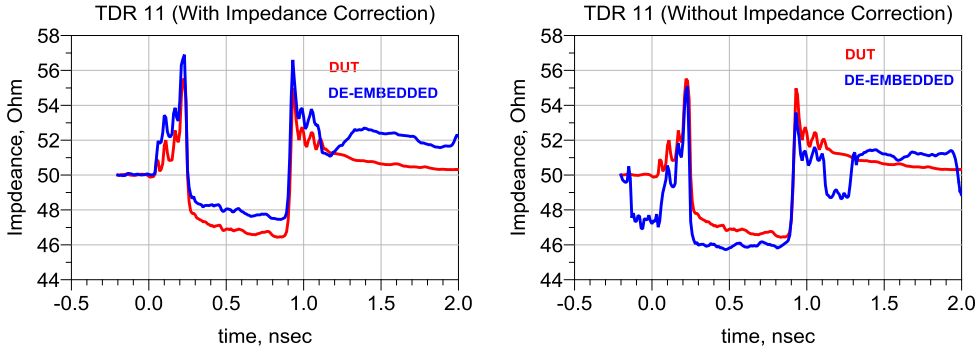

Figure 35: Comparison of de-embedded TDR profile with impedance correction (left) and without impedance correction (right) in the de-embedding algorithm.

Apart from the examples shown above, there are multiple other combinations to stress the de-embedding algorithms like using an asymmetric test fixture [22] or creating a impedance profile difference on the connector transition by incorrectly assembling the edge mounted connectors as shown in Figure 36.

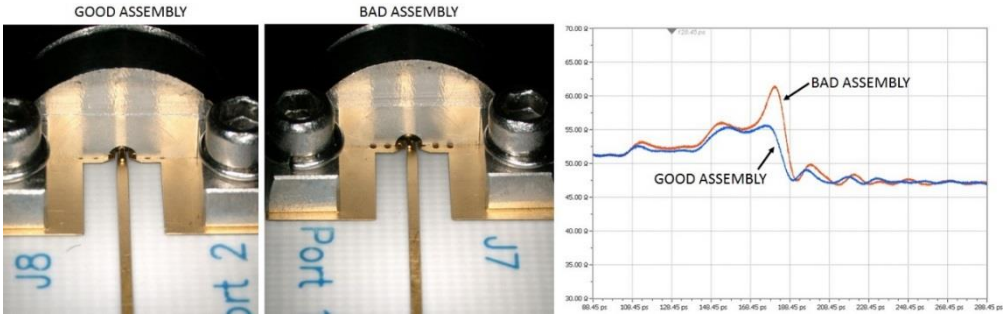

Figure 36: Degrading the connector transition by incorrectly assembling the edge connector.

Differential Coupled Kit

To extend the single-ended kit to a differential kit, one could just simply duplicate the number of test coupons in Figure 11 creating a differential PCB kit. But this would be a non-coupled differential kit. A non-coupled differential kit does not stress the de-embedding algorithm as a strongly coupled differential kit would. Because of this fact, the proposed differential kit for evaluating de-embedding algorithms is composed of coupled structures as shown in Figure 37. This kit was implemented on a Nelco 4000-13 SI dielectric with silver plating.

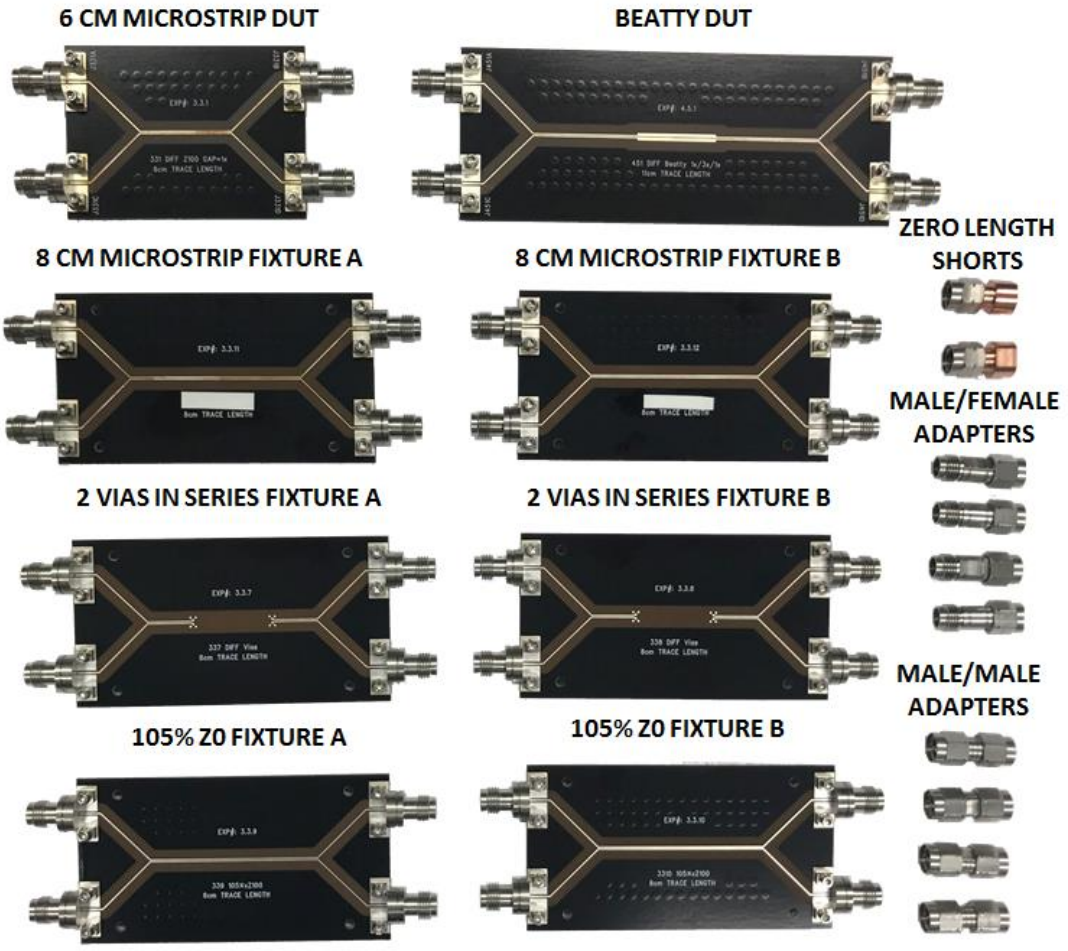

Figure 37: Differential kit picture.

The measurement methodology for the test fixture and DUTs is the same as on the single-ended case although the number of connectors and adapters are double. This makes connecting all the PCB modules and adapters a little bit tricky as shown in Figure 38, Figure 39, Figure 40 and Figure 41.

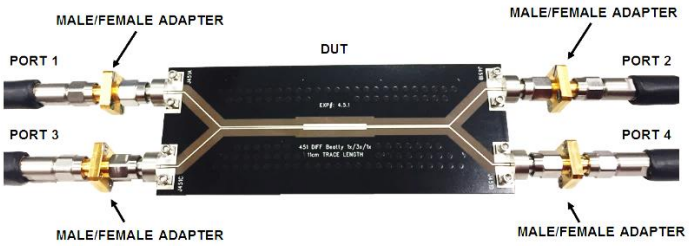

Figure 38: Setup example picture for measuring the DUT.

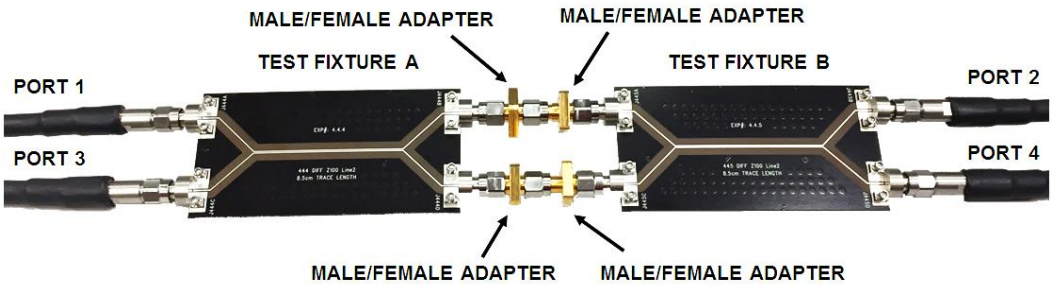

Figure 39: Setup example picture for measuring the test fixture 2x-thru.

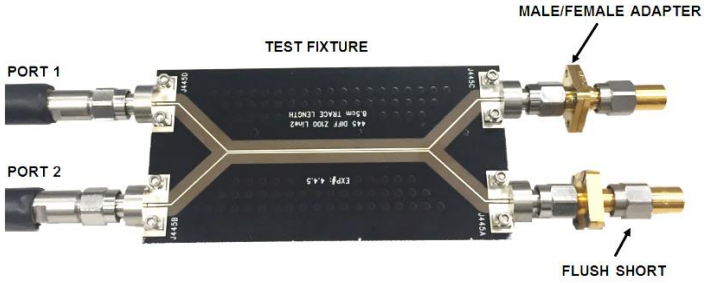

Figure 40: Setup example picture for measuring the open/short 1x-reflect (short on the picture).

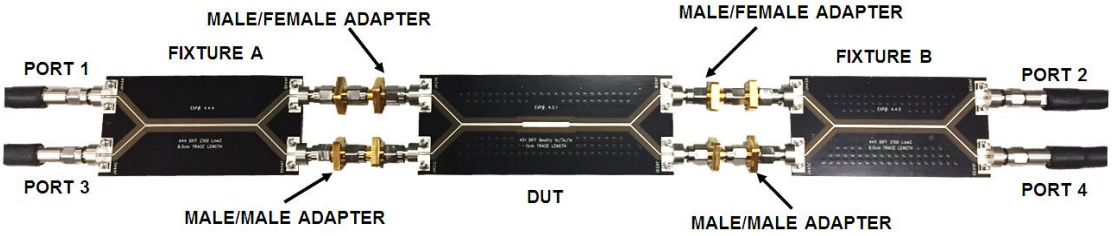

Figure 41: Setup example picture for measuring the DUT plus the test fixture.

Figure 42 shows the measured differential insertion and return loss for the 2x-thru composed of two differential microstrip coupons. Figure 42 also shows the single-ended insertion loss of the 2x-thru, clearly showing that the differential pair is coupled. Figure 43 shows the differential insertion and return loss for the test fixture plus DUT for the 6 cm microstrip and Beatty standard DUTs with the microstrip test fixture.

Figure 44 presents the de-embedding results and the corresponding error metrics for the 6 cm microstrip DUT case and Figure 45 for the differential Beatty DUT.

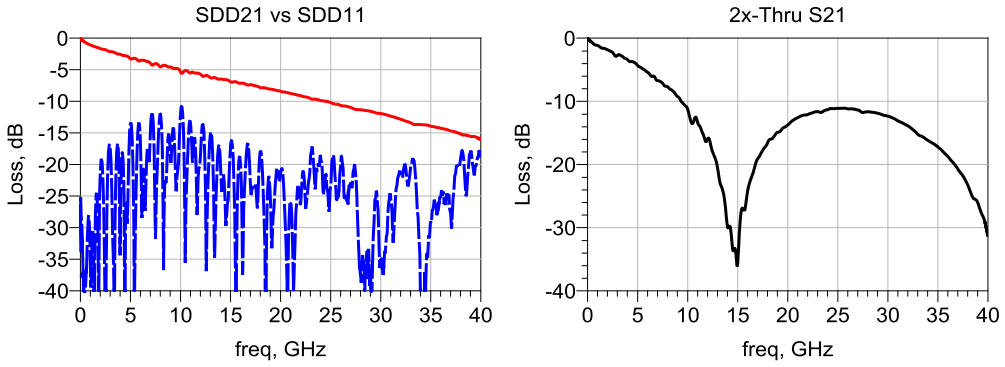

Figure 42: Measured differential insertion (SDD21) and return (SDD11) loss (left) and single-ended insertion loss (right) for the 2x-thru composed of the two differential microstrip traces.

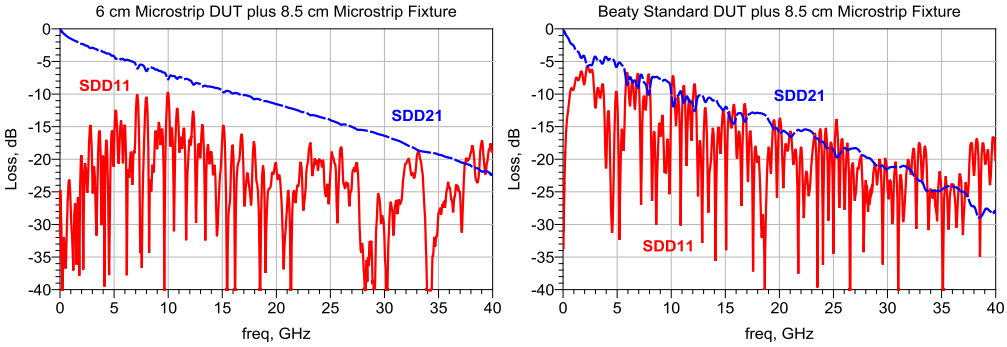

Figure 43: Measured differential insertion (SDD21) and return (SDD11) loss for the 6 cm differential microstrip DUT (left) and differential Beatty DUT (right) with the differential microstrip test fixture.

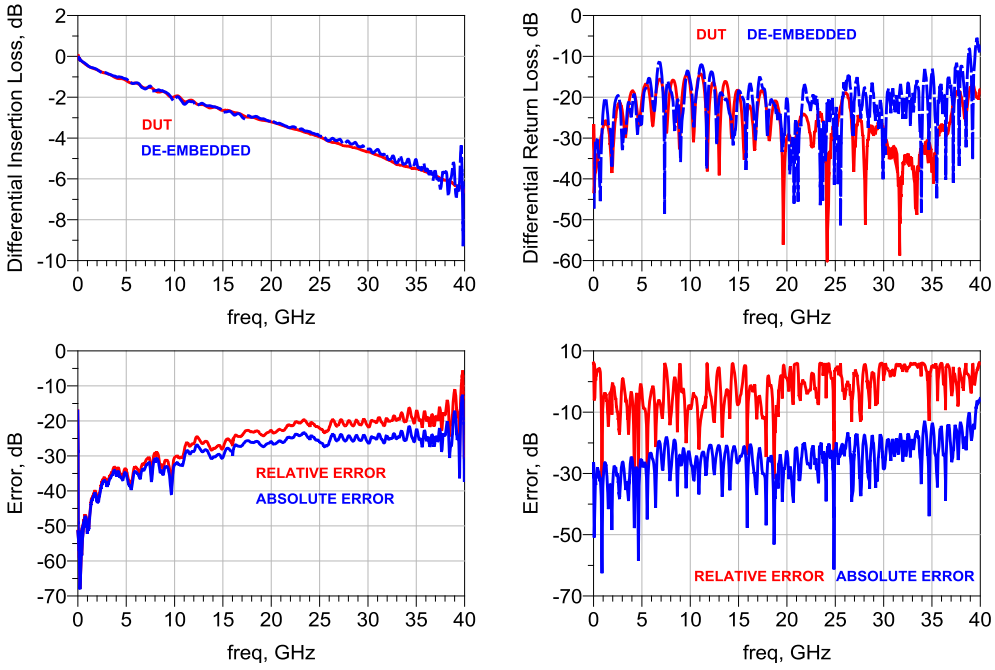

Figure 44: De-embedding results using a 2x-thru de-embedding algorithm for the 6 cm differential microstrip DUT with the differential microstrip test fixture.

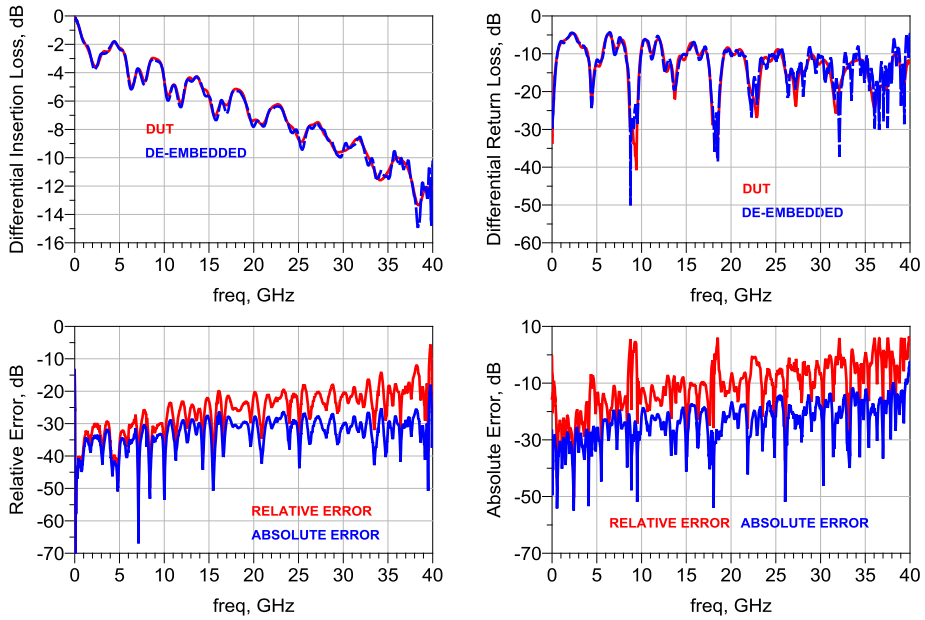

Figure 45: De-embedding results using a 2x-thru de-embedding algorithm for Beatty standard DUT with the differential microstrip test fixture.

Crosstalk De-Embedding Evaluation Kit

In test fixture designs with signal traces in close proximity in the test fixture, removing the fixture crosstalk is challenging [25]. Although de-embedding algorithms like 2x-thru can de-embed the loss in multiport setups, the fixture crosstalk removal is often ignored to avoid the complexity in the de-embedding algorithm. This can result on the measured crosstalk from the DUT to be higher than its real value. In order to measure DUT crosstalk properly, the fixture crosstalk need to be fully de-embedded or to be quantified. In order to quantify the fixture crosstalk which remains after a calibration or de-embedding, the dogleg/ spiderleg structure has been proposed [25]. For a de-embedding algorithm which is equipped with the fixture crosstalk removal, the dogleg/spiderleg can also serve as the 2x-thru de-embedding structure.

Figure 46 shows two 8-port test coupons which have been developed to validate the fixture crosstalk removal of a de-embedding algorithm that also de-embeds crosstalk.

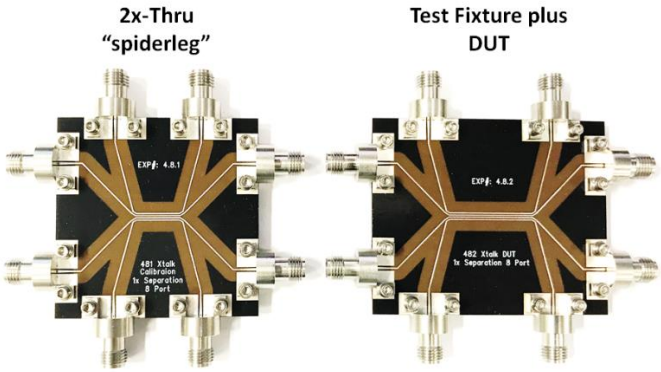

Figure 46: Crosstalk de-embedding verification test fixtures.

The test coupons are composed of four traces of which spacing is narrowed as the traces approach to the center from the launch connectors. In the middle of the routing, the spacing is kept constant for a certain length. The PCB dielectric material is Nelco 4000-13 SI. The trace width is 11.6 mil. The edge-to-edge spacing between traces is also 11.6 mil in the middle. The test coupon on the left in Figure 43 is the 2x-thru de-embedding structure which is so called the spiderleg. The coupling region at the center is 1 cm long. The test coupon on the right, represents the test fixture plus the DUT. The coupled region is 2 cm long. Hence the DUT is the four coupled traces of 1 cm long.

Figure 47 shows the measured differential FEXT and NEXT of the two test coupons. The FEXT results show the clear increase of the crosstalk for the test fixture with the DUT when compared with the spiderleg 2x-thru coupon. The challenge for the de-embedding algorithm is then to de-embed not only the loss but also the test fixture crosstalk so that only the crosstalk due to the 1 cm DUT is presented on the S-parameters. In this paper, we do not present a deep analysis of the structures including an estimation of the DUT crosstalk based on measurement based modeling, which is needed to assess the accuracy of the de-embedding algorithm under analysis. On this section, we only presented a 8-port case (e.g. two differential traces), but the same philosophy and the framework is still valid to the crosstalk de-embedding and its verification for 4-port/ 12-port VNA measurements and beyond. This will be presented in a future paper together with the detailed verification.

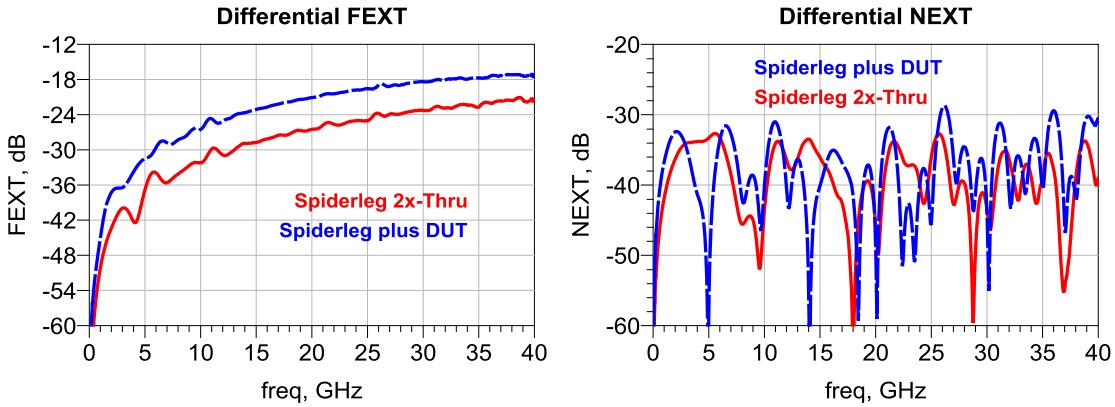

Figure 47: Measured differential FEXT and NEXT for the spiderleg coupon and for the test fixture plus DUT coupon.

S-Parameters Quality

Obtaining a S-parameter set from a de-embedding algorithm using the presented methodology with a small error does not guarantee that the S-parameter set has a high quality in terms of passivity and causality [26]. This will depend on the initial measured data but also on the de-embedding algorithm. Any data that is available for describing a physical system is not perfectly accurate and does not describe it comprehensively. Measurements always have noise from various sources, the results are band limited and can only be obtained at a finite discrete set of points. Usually de-embedding algorithms are very sensitive and these errors can be amplified after de-

embedding. Some de-embedding software packages also enforce passivity and causality for generated de-embedding data. It becomes important to be able to estimate the quality of existing data in order to achieve reliability of the results and conclusions developed based on it This is also an important topic on the IEEE P370 standard development [8].

One of the most important properties of the S-Parameters is causality. Causality is a property of a physical system that reflects an intuitive notion of cause and consequence. Specifically, no system output can be observed before the input was applied. Causality violation of a raw data can significantly impact de-embedding procedure. Most de-embedding algorithms include two steps: First part is related with obtaining fixture S-Parameters from 2x-thru and the second one is related with removing fixture effect from fixture + DUT + fixture measurement. The algorithm of the first part includes time domain pealing, which means that two fixtures should be separated in the time domain. In this case, causality of the data is very important. If the second fixture violates causality property and starts before the effect from the first fixture ends, then information from two fixtures will be mixed and accurate fixture separation will be extremely difficult.

The second part of the de-embedding algorithm removes the test fixture, obtained by splitting 2x-thru structure, from fixture+DUT+fixture measurement. Usually the 2x-thru structure and test fixture attached to the DUT are not identical due to manufacturing process variations. If this difference is significant, then S-Parameters of the de-embedded DUT will have causality violation. Some de-embedding software packages are correcting extracted fixture to compensate this difference and avoid non-causality issues in the de-embedded DUT.

Another important property of S-Parameters is passivity. Passivity is a property of a network which does not generate energy. Passivity is an important property for de-embedding algorithms. De-embedding is an inverse operation of cascading. Let's assume that 2x-thru is a cascading of left and right fixtures. Then S21 of the 2x-thru can be calculated using the following formula:

$$S_{21}^{2x} = \frac{S_{21}^{Left} S_{21}^{Right}}{1 - S_{22}^{Left} S_{11}^{Right}}$$

Numerator of this formula describes multiple reflections between left and right fixtures and represents the following series of infinite geometric progression:

$$1 + S_{22}^{Left} S_{11}^{Right} + \left(S_{22}^{Left} S_{11}^{Right}\right)^2 + \left(S_{22}^{Left} S_{11}^{Right}\right)^3 + \cdots$$

This geometric progression is converging to the numerator of the cascading formula if and only if absolute value of $S_{22}^{Left} S_{11}^{Right}$ is less or equal to one. If S-Parameters of the left and right fixtures violates passivity property, then convergence criteria might not be satisfied and all formulations used in de-embedding algorithms will be wrong.

From the above it follows that it is very important to have a metric estimating S-Parameters quality based on passivity and causality. In [8,27,28] a metric that estimates passivity, causality and reciprocity properties in physical units is presented. The estimation procedure is the following: First passive, causal and reciprocal models are created based on original data and then difference in time domain is estimated. This estimation has a physical meaning and is a maximum difference that can be obtained between original and enforced time domain waveforms if the worst bit sequence will be used as an input signal.

Conclusions

This paper has presented a PCB kit that can be used to evaluate the accuracy of a de-embedding algorithm using the 2x-thru or 1x-reflect methodologies. Simulation based S-parameters libraries allow easy exploration of the impact of single parameters have on the de-embedding algorithms accuracy. The presented PCB kit and methodology does not provide that kind of flexibility but instead brings a series of other important real life components to evaluate a de-embedding algorithm including the measurement setup. Both approaches are needed in the evaluation of a de-embedding algorithm. The presented PCB kit is only a small subset of the possible DUT and test fixture combination that one can think.

Another important usage of the presented PCB is as an introduction and training vehicle for S-parameter de-embedding. Most S-parameters de-embedding users see the de-embedding process as a black box or even never use it. This PCB kit and methodology allows them to learn and understand the requirements and limitations for a successful S-parameter de-embedding.

Acknowledgments

We would like to thank Bill Rosas from Signal Microwave and Brian Shumaker from DVT solutions for commercializing the single-ended kit and making it available to the engineering community. Evan Green and R&D Altanova for the design and manufacturing of the differential and crosstalk kits and Lisa Ward from Rohde and Schwarz for her support.

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